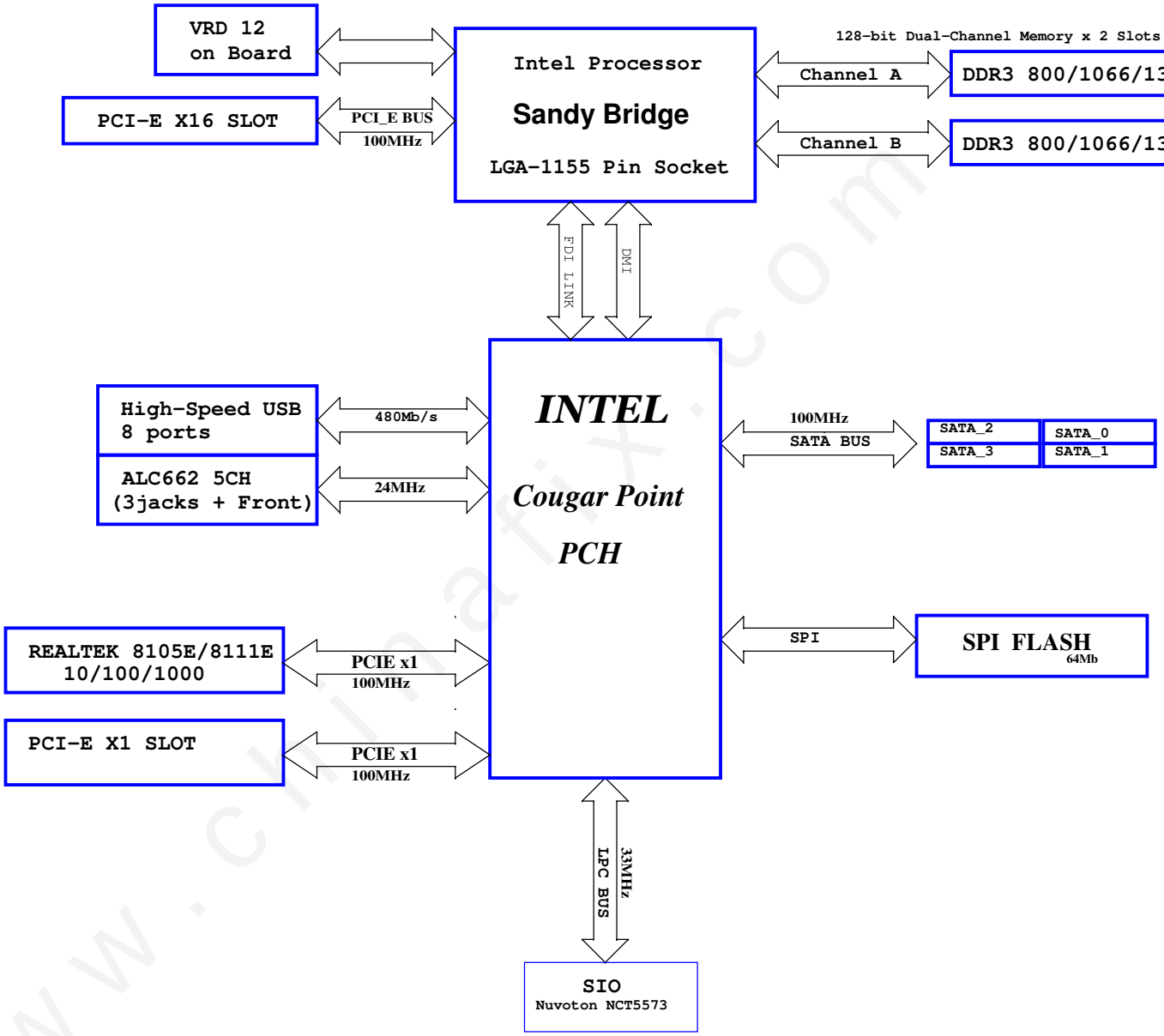
H67M-VS3 R1.02
H61M-VG3 R1.02

Draft



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H67M-ITX

ASRock Title : Block Diagram

ASRock Inc. Engineer: Isaac Lee

Size	Project Name	Rev
A3	H67M-ITX	1.03

Date: Tuesday, May 07, 2013 Sheet 1 of 47

Schematics Change History

Version	Date	Comments
H61M-VS3 1.00	2012/09/14	Primary release

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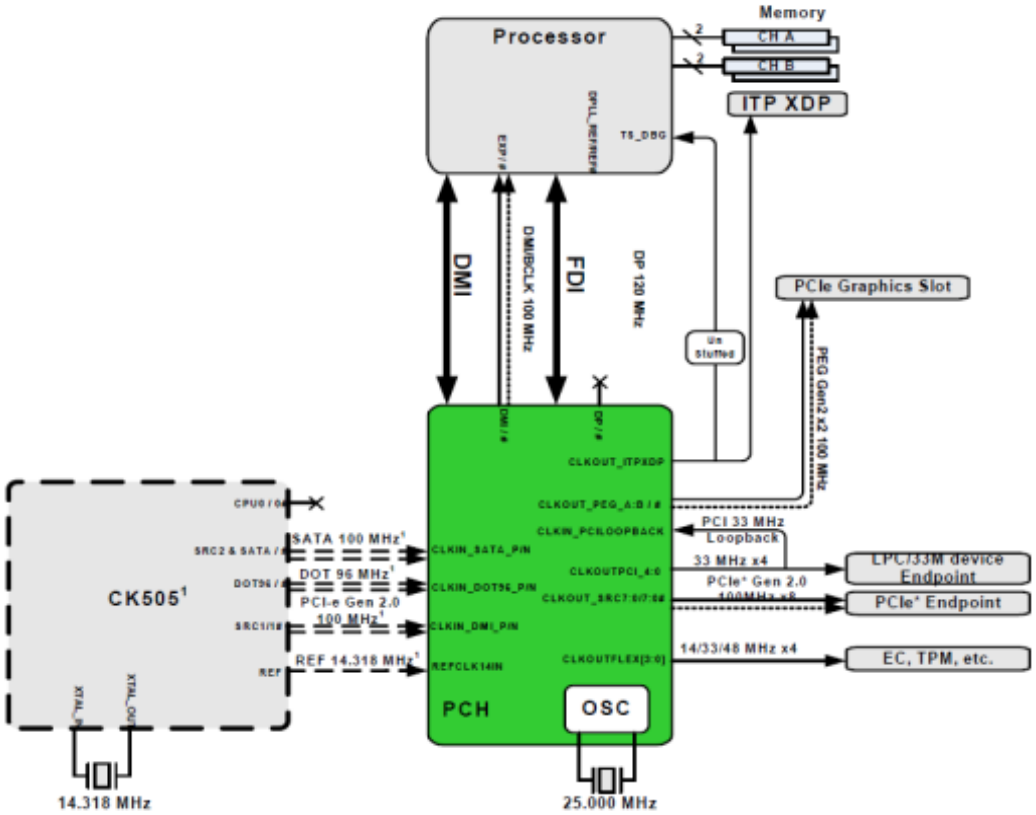
Full Integrated Clock Mode



1. CK505 and PCH input clock sources indicated are Buffer Through mode back-up routes only and can be un-stuffed when in full clock integration mode

H67M-ITX

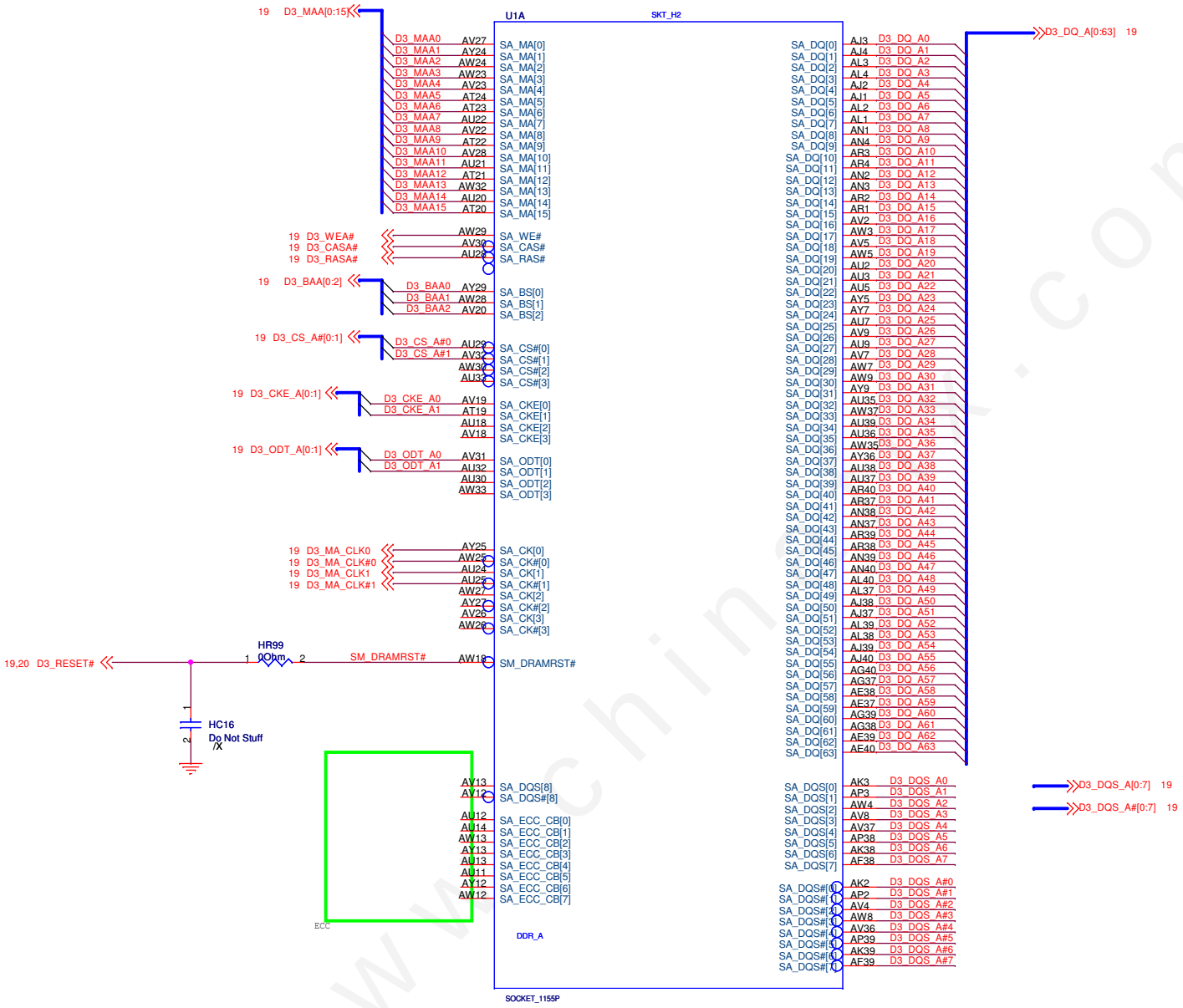
ASRock Title : Clock Distribution

ASRock Inc. Engineer: Isaac Lee

Size	Project Name	Rev
A3	H67M-ITX	1.03

Date: Wednesday, December 19, 2012 Sheet 3 of 47

NO DATA MASK (DM) on Sandy Bridge Memory Controller!!
Tie DM signals to GND in the DIMM side!!



H67M-ITX

ASRock Title : MEM CTRL CHA

ASRock Inc. Engineer: Isaac Lee

Size	Project Name	Rev
A3	H67M-ITX	1.03

Date: Wednesday, December 19, 2012 Sheet 4 of 47

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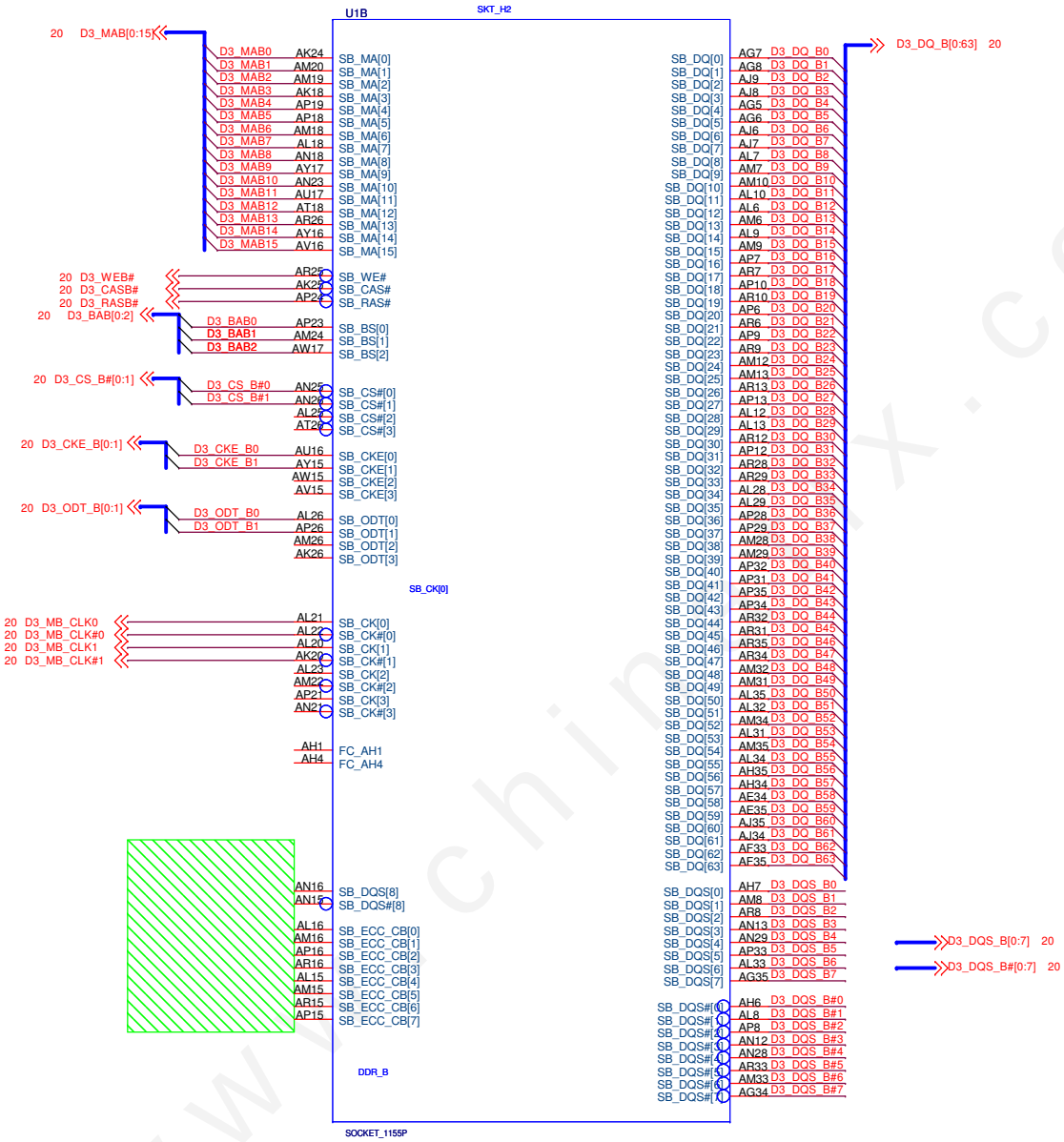
NO DATA MASK (DM) on Sandy Bridge Memory Controller!!
Tie DM signals to GND in the DIMM side!!



H67M-ITX

ASRock Inc.

Title : MEM CTRL CHB

Engineer: Isaac Lee

Size	Project Name	Rev
A3	H67M-ITX	1.03

Date: Wednesday, December 19, 2012 Sheet 5 of 47

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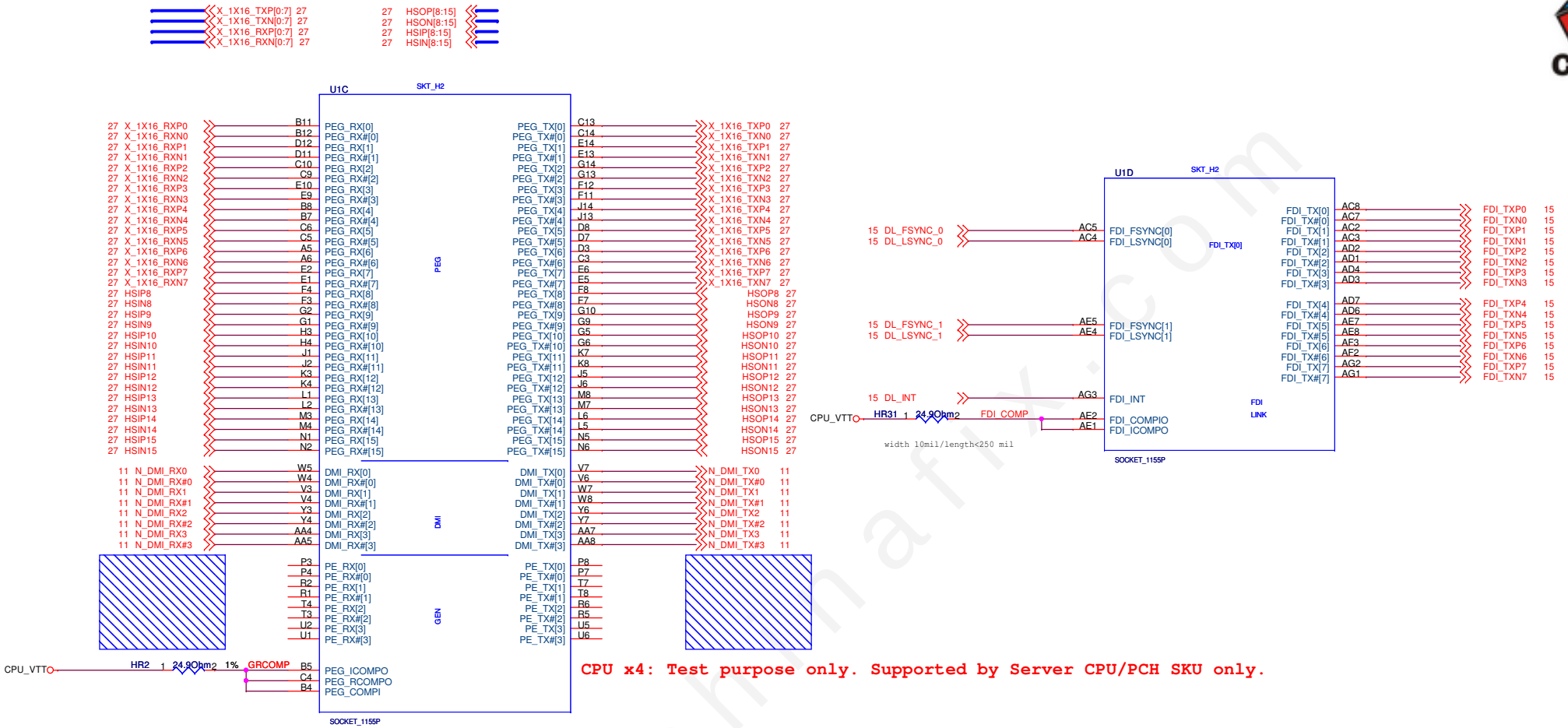
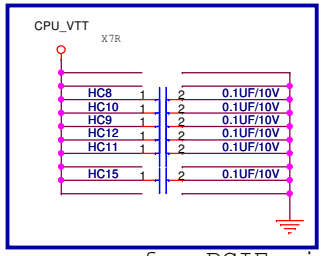


CPU x4: Test purpose only. Supported by Server CPU/PCH SKU only.

GRCOMP<500mil
U1.B4 and U1.C4 tight together then use 4 mil trace to HR2.2
U1.B5 use 10 mil trace separate to HR2.2



for PCIE signal trans-layer decoupling capacitors!!!
Place near trans-layer vias for PCIe lanes.

H67M-ITX

ASRock Inc.

Title : CPU - PEG/FDI

Engineer: Isaac Lee

Size	Project Name	Rev
A3	H67M-ITX	1.03

Date: Wednesday, December 19, 2012 Sheet 6 of 47

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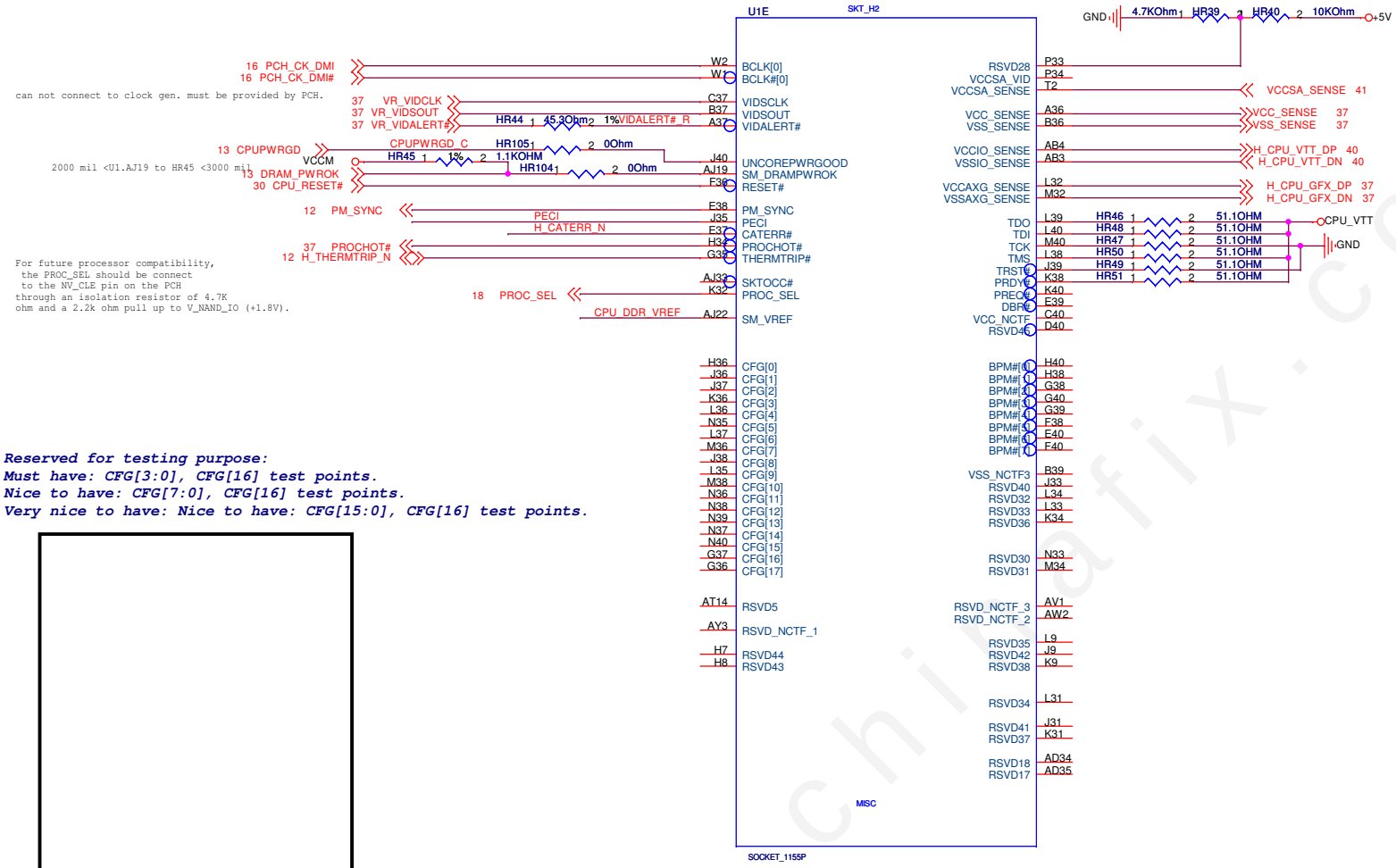
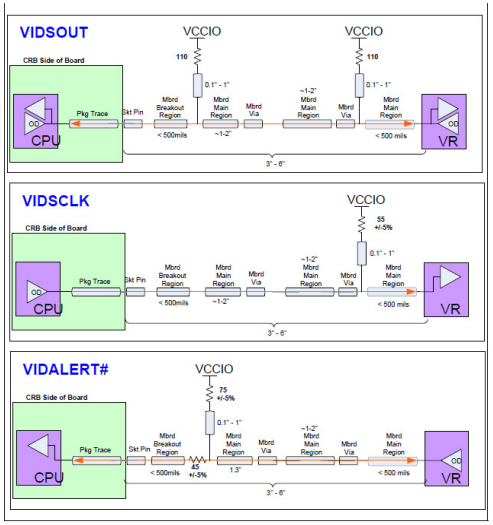
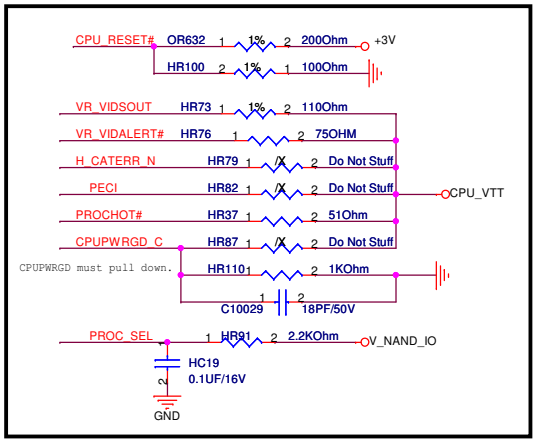
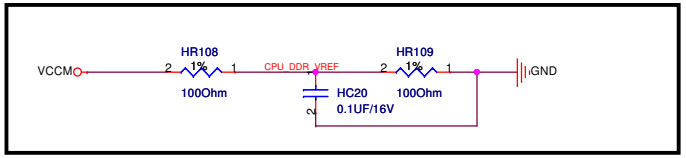


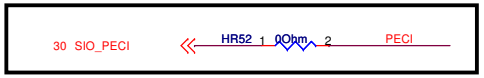
SVID Placement needs to pay attention for pull up resistors. See PDG page 300



Reserved for testing purpose:
Must have: CFG[3:0], CFG[16] test points.
Nice to have: CFG[7:0], CFG[16] test points.
Very nice to have: Nice to have: CFG[15:0], CFG[16] test points.







H67M-ITX

ASRock Inc.

Title : CPU-MISC

Engineer: Isaac Lee

Size	Project Name	Rev
A3	H67M-ITX	1.03

Date: Wednesday, December 19, 2012 Sheet 7 of 47

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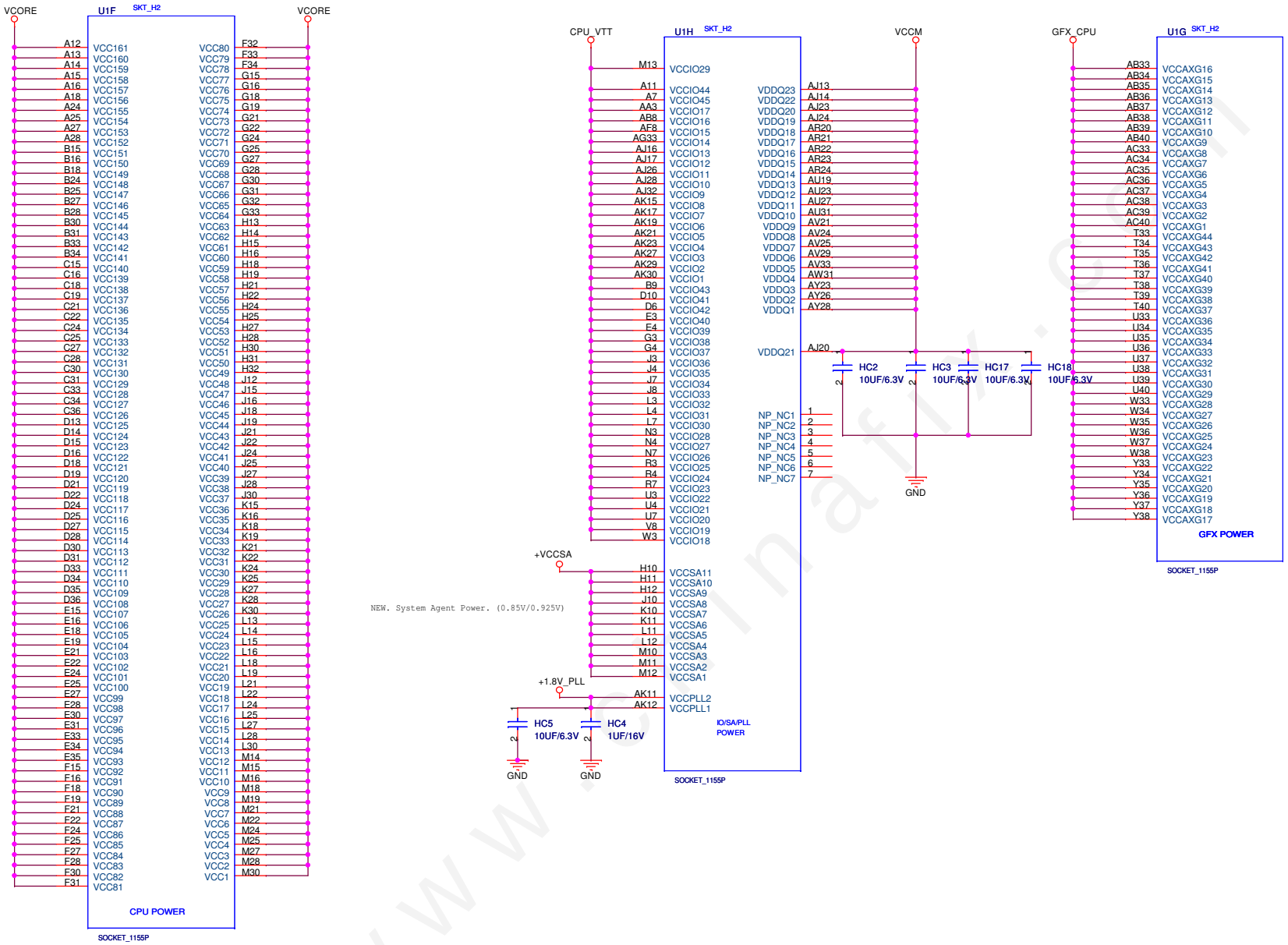

H67M-ITX

ASRock Title : CPU - Power

ASRock Inc. Engineer: Isaac Lee

Size	Project Name	Rev
A3	H67M-ITX	1.03

Date: Wednesday, December 19, 2012 Sheet 8 of 47

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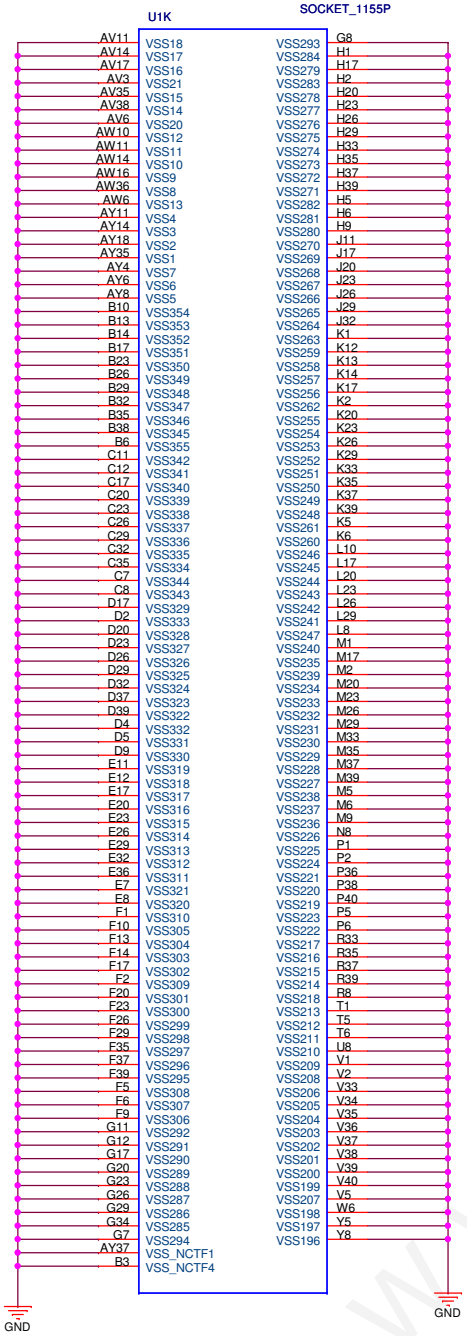
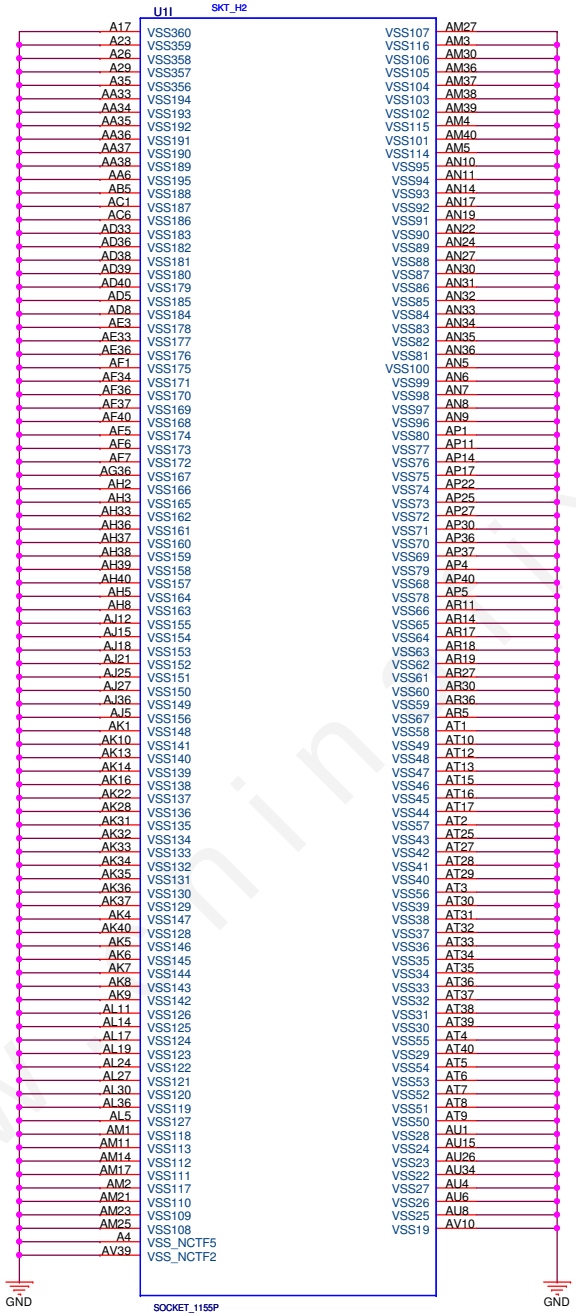
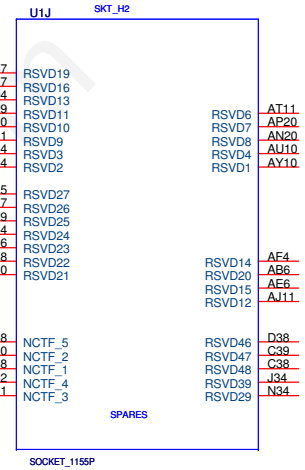
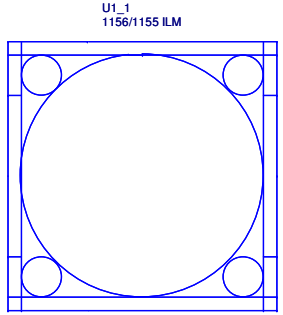




All reserved. No connected.





H67M-ITX

ASRock Title : CPU - GND

ASRock Inc. Engineer: Isaac Lee

Size	Project Name	Rev
A3	H67M-ITX	1.03

Date: Wednesday, December 19, 2012 Sheet 9 of 47

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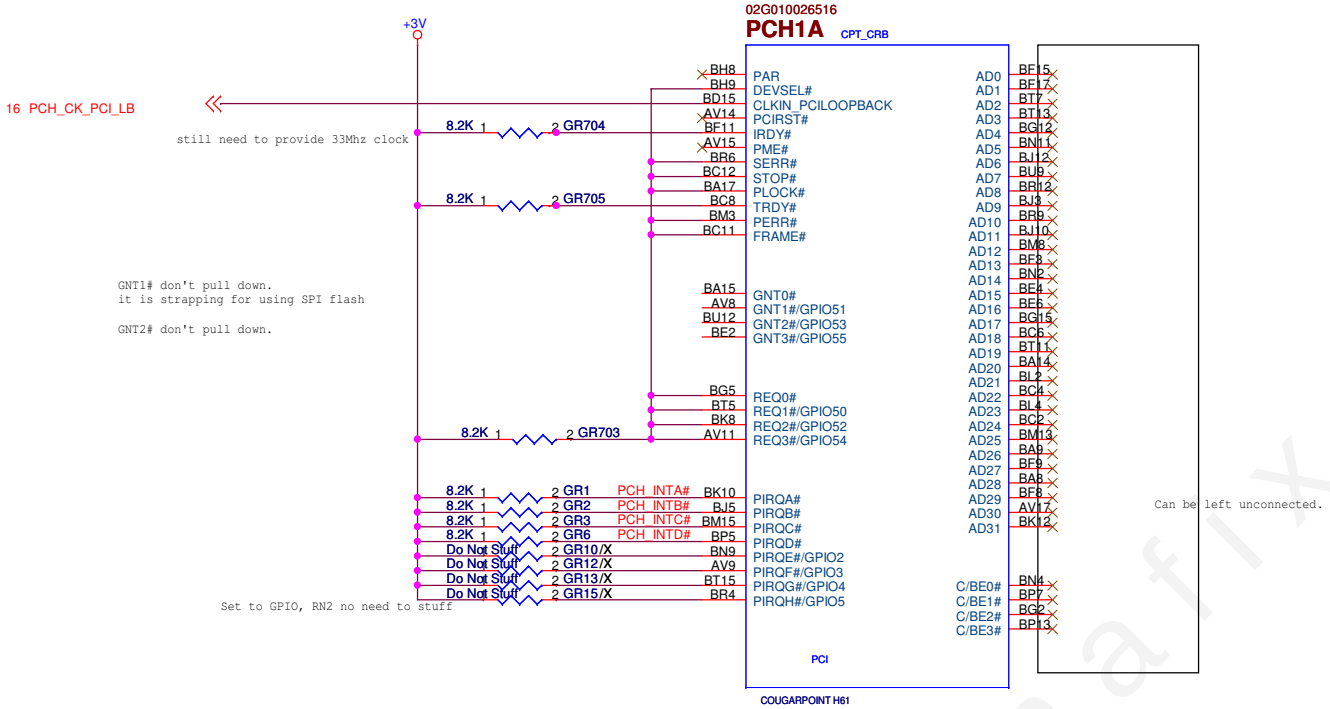
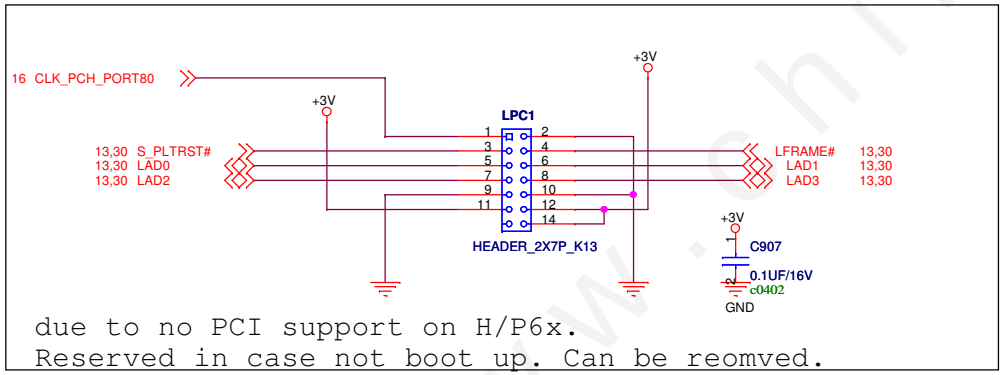
H67/P67 do not support PCI. Check PCI solution!!!





due to no PCI support on H/P6x.
Reserved in case not boot up. Can be reomved.

H67M-ITX

ASRock Inc.	Title : PCH - PCI/LPC	
	Engineer: Isaac Lee	
Size B	Project Name H67M-ITX	Rev 1.03
Date: Tuesday, May 07, 2013	Sheet 10 of 47	

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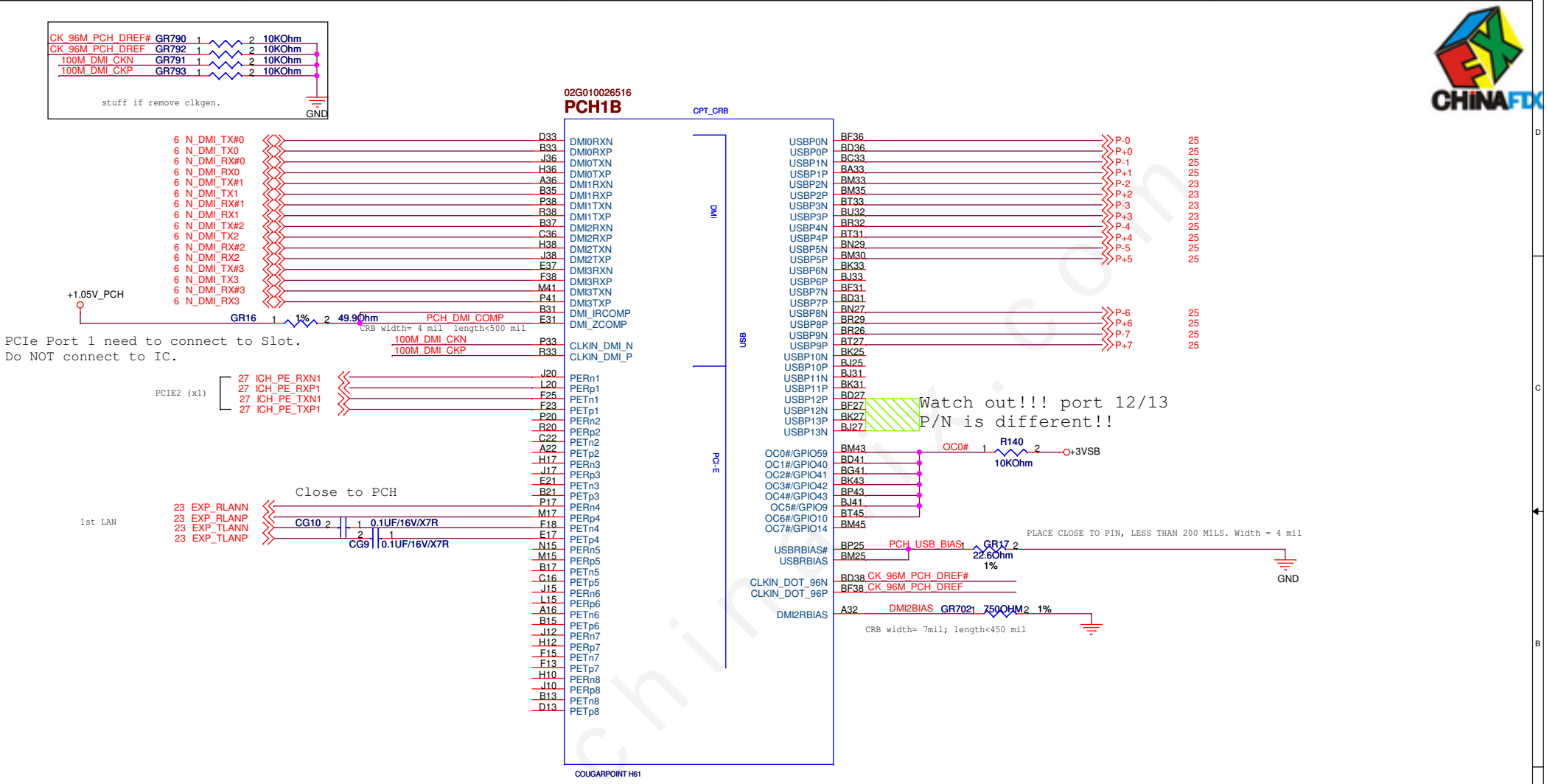


H67M-ITX

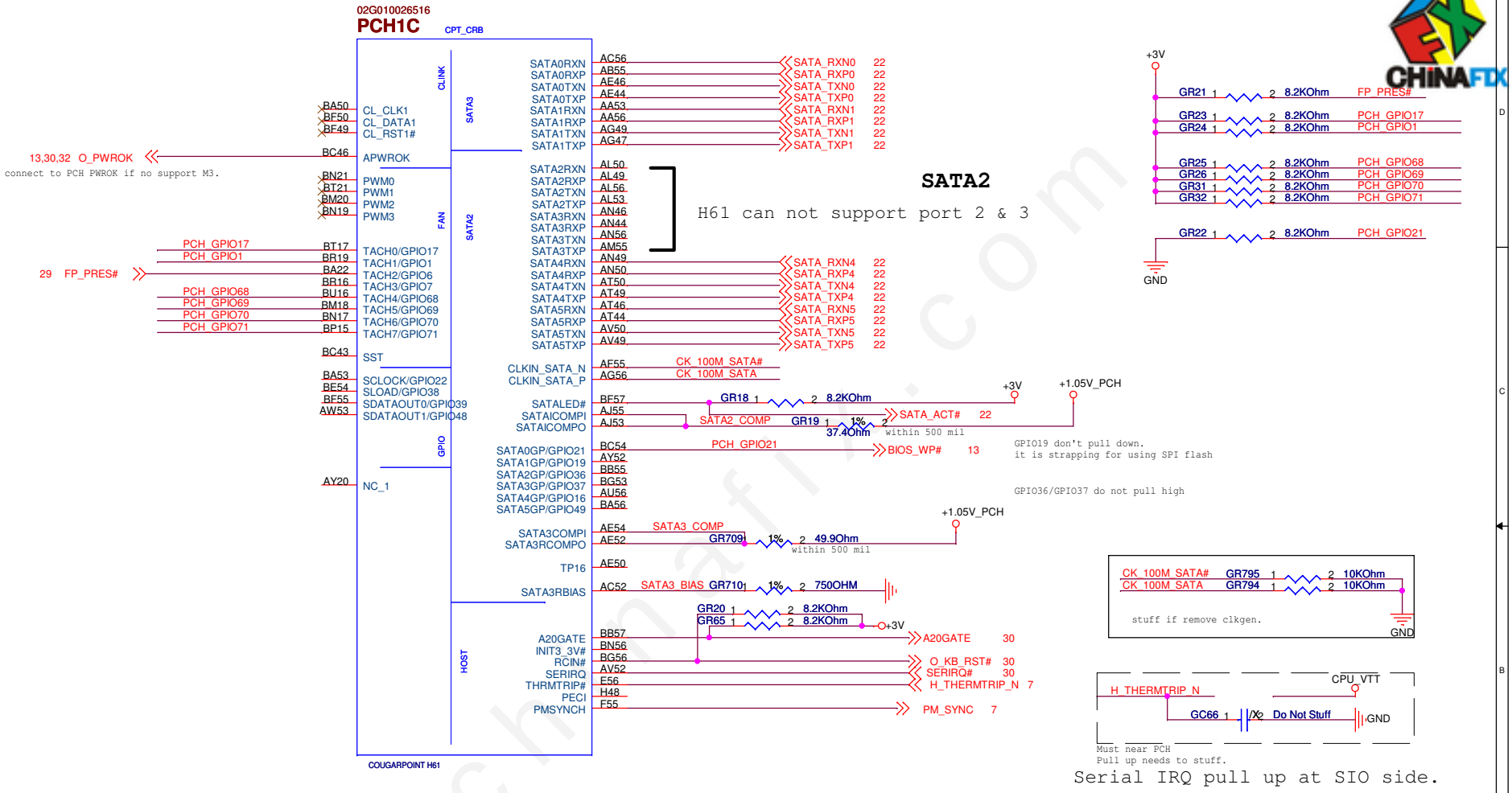
ASRock Inc.

Title : PCH - PCIE/DMI/USB

Engineer: Isaac Lee

Size	Project Name	Rev
B	H67M-ITX	1.03

Date: Tuesday, May 07, 2013 Sheet 11 of 47



H67M-ITX

ASRock Inc.	Title : PCH - SATA/HOST	
	Engineer: Isaac Lee	
Size B	Project Name H67M-ITX	Rev 1.03
Date: Tuesday, May 07, 2013	Sheet 12 of 47	

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	HIGH	LOW
GPIO8(IPU)	BTM	FCIM

Enable Internal VRM

GPIO28	High
HDA_SYNC	Low

02G010026516

PCH1D

COUGARPOINT H61

Pull High/Low

Flash descriptor overide

DPWROK DELAY

+3VSB_A

GR726 100KOhm

DPWROK

GC72 1UF/16V

GND

FET Control

ATX+5VSB

GR776 8.2KOhm

GR778 220KOhm

SLP_SUS_FET

GQ17 PMBS3904

GR777 220KOhm

SLP_SUS#

GC801 1UF/6.3V

GC802 1UF/6.3V

GND

unstuff all if using SIO's function!

Q811 Do Not Stuff

R8487 0Ohm

SLP_SUS_FET_1

+5VSB

+3VSB_A

Q812 Do Not Stuff

R8491 0Ohm

+3VSB

SPI ROM

F1_SPI_CS#_R — F1_SPI_CS#

F1_SPI_MOSI_R — F1_SPI_MOSI

F1_SPI_MISO — F1_SPI_MISO

F1_SPI_CLK_R — F1_SPI_CLK

SPI_MOSI do not pull high

U3_1 SPI 32Mb

BIOS_WP# GR7 0Ohm

GC2 0.1UF/16V

GR4 8.2KOhm

GR5 8.2KOhm

U3 SOCK8

F1_SPI_CS# / F1_SPI_MISO / R_SPI_WP#

SPI_HOLD1# / F1_SPI_CLK / F1_SPI_MOSI

GC3 0.1UF/16V c0402

GC65 0.1UF/16V c0402

RTC

S_ICH_RTCX1 — GR14 10MOhm — S_ICH_RTCX2

GY1 32.768KHZ

GC5 10PF/50V

GC6 10PF/50V

S_SRST# — GC4 1UF/10V c0603

GY1_1 JUMPER_WIRE 0.5*6.3*4*6.3mm

RTCX1 and RTCX2 width=4,Length=<1

Case Open

CI1 HEADER_1X2P

CASEOPEN — S_INTRUDER#

OC1 0.1UF/16V

GND

H67M-ITX

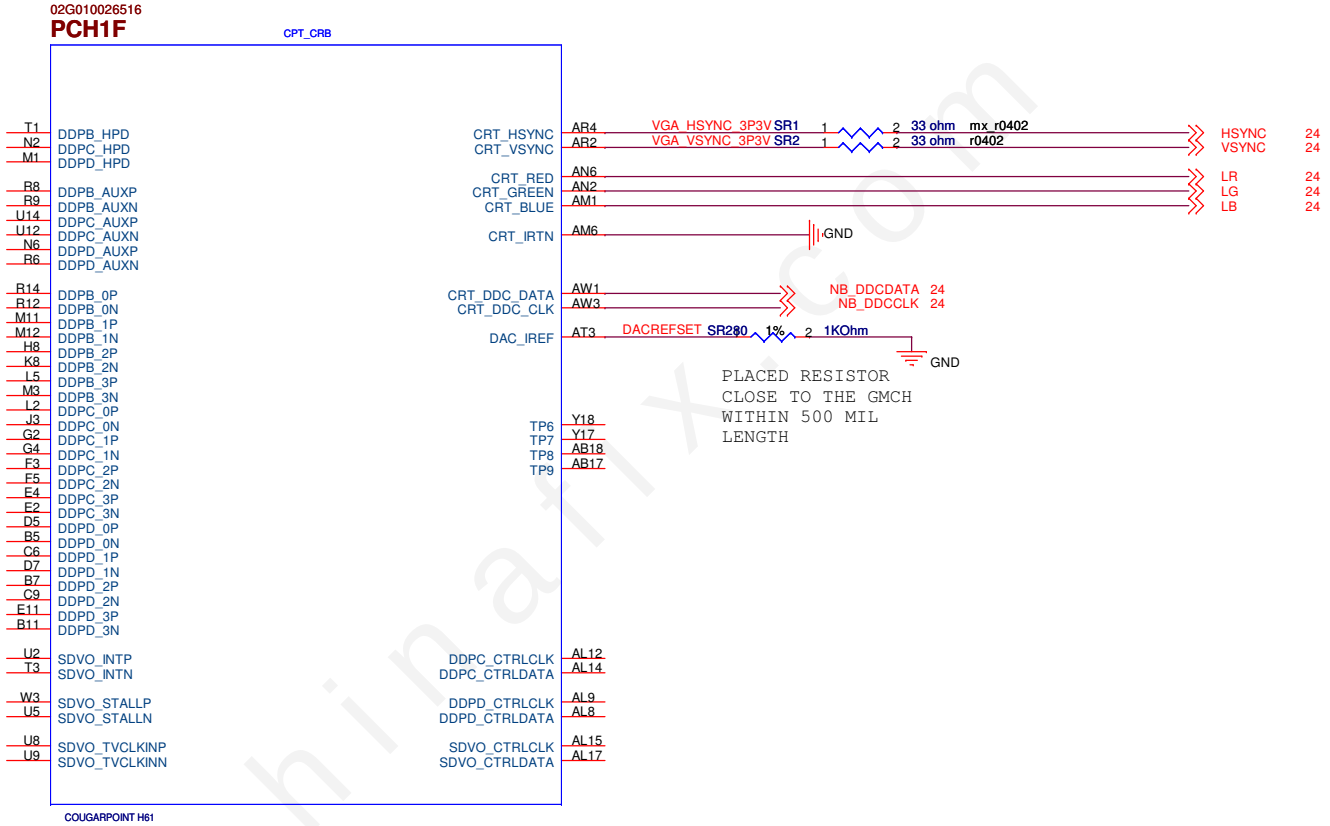
ASRock Inc.

Title : Audio/MISC

Engineer: Isaac Lee

Size	Project Name	Rev
Custom	H67M-ITX	1.03

Date: Monday, December 24, 2012 Sheet 13 of 47



All AC couple capacitors
put in the connector side.

- In an effort to address customer display issues more efficiently Intel recommends customers adopt digital display configuration similar to Intel CRB as following

Digital Port	Display Technology
Port B	DVI or SDVO (Desktop) DisplayPort, HDMI/DVI or SDVO (Mobile)
Port C	DisplayPort (Desktop) DisplayPort/HDMI/DVI (Mobile)
Port D	HDMI/DVI/eDP* (Desktop) HDMI/DVI/DisplayPort (Mobile)

H67M-ITX

ASRock Title : PCH - Display

ASRock Inc. Engineer: Isaac Lee

Size	Project Name	Rev
B	H67M-ITX	1.03

Date: Tuesday, May 07, 2013 Sheet 14 of 47

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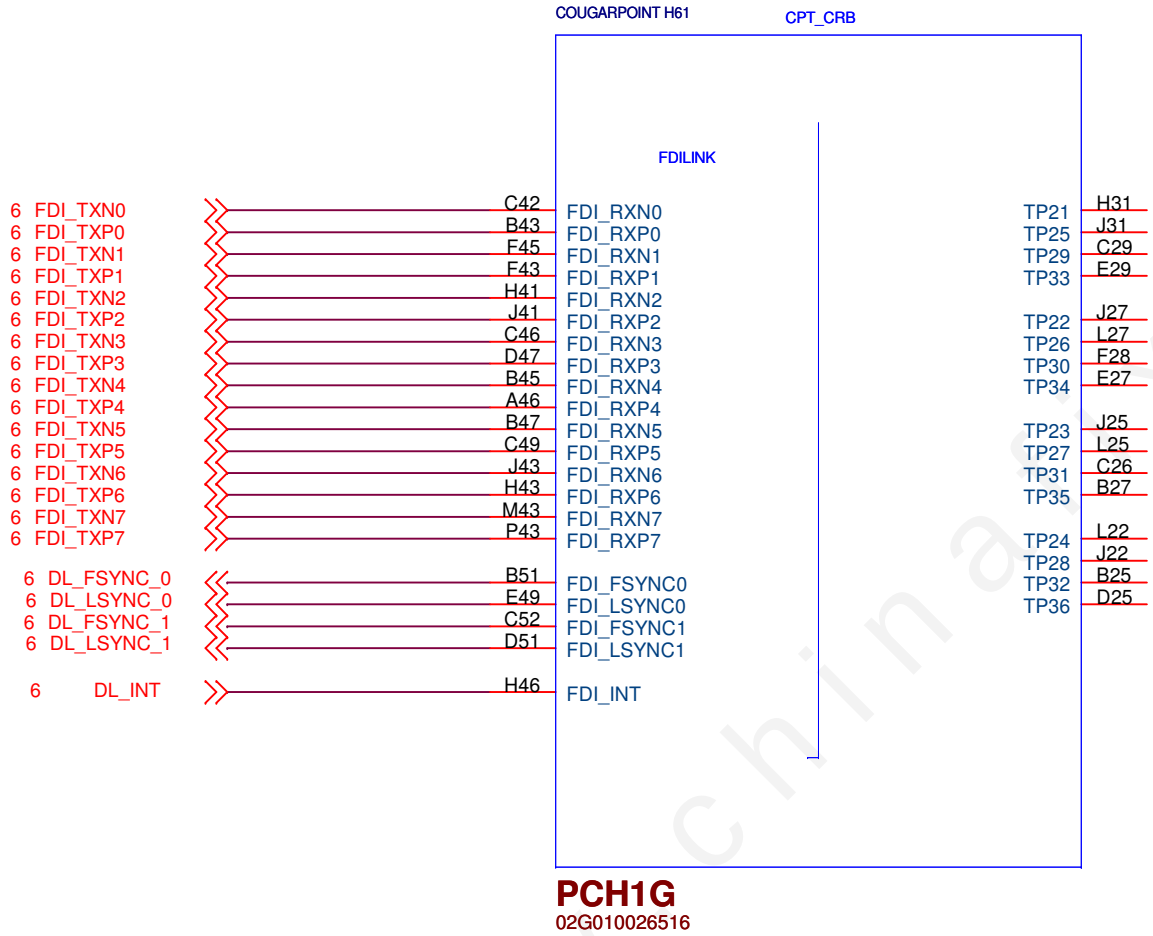

H67M-ITX

ASRock Inc.	Title : PCH - FDI	
	Engineer: Isaac Lee	
Size: A	Project Name: H67M-ITX	Rev: 1.03
Date: Tuesday, May 07, 2013	Sheet 15 of 47	

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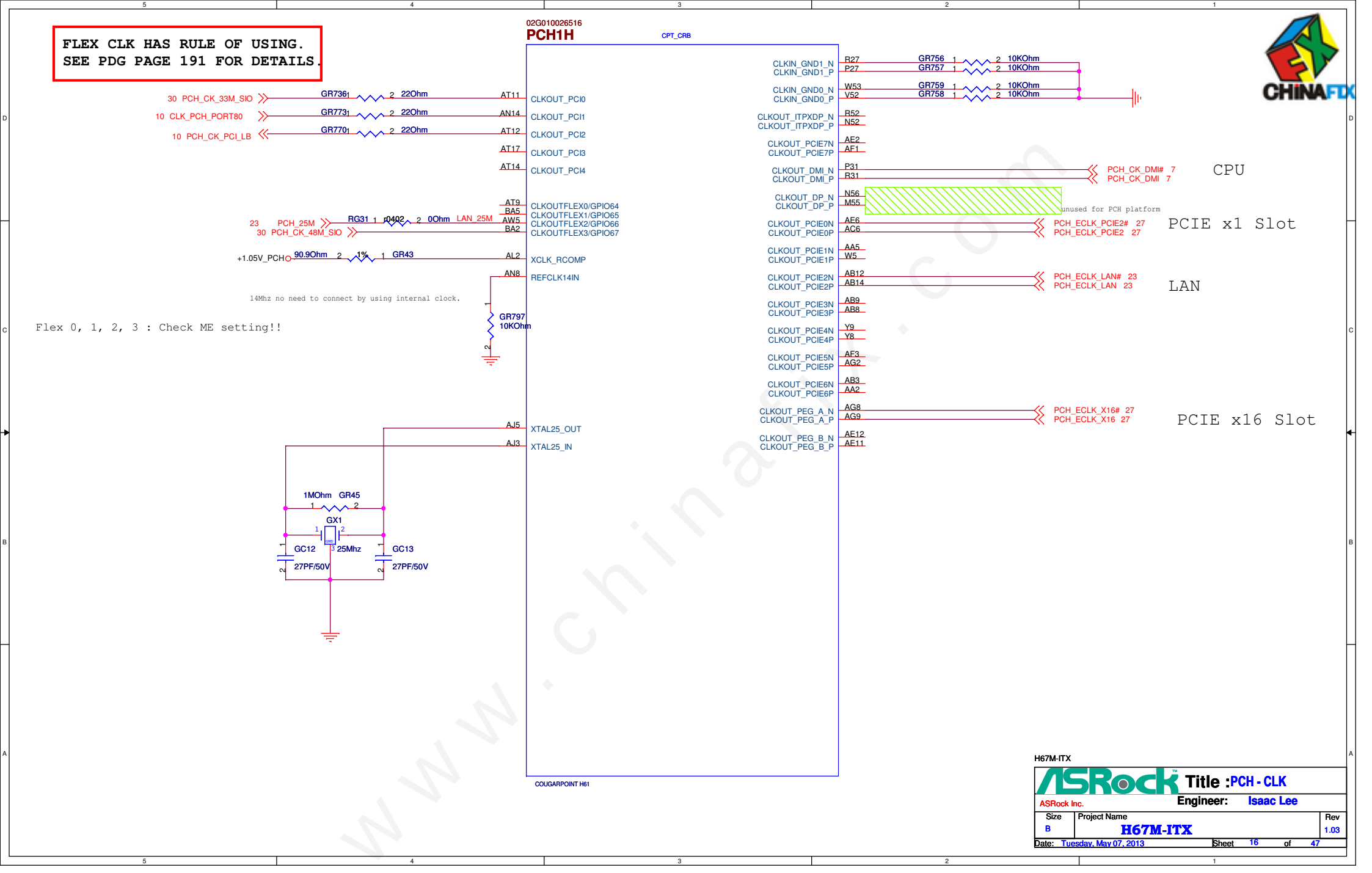
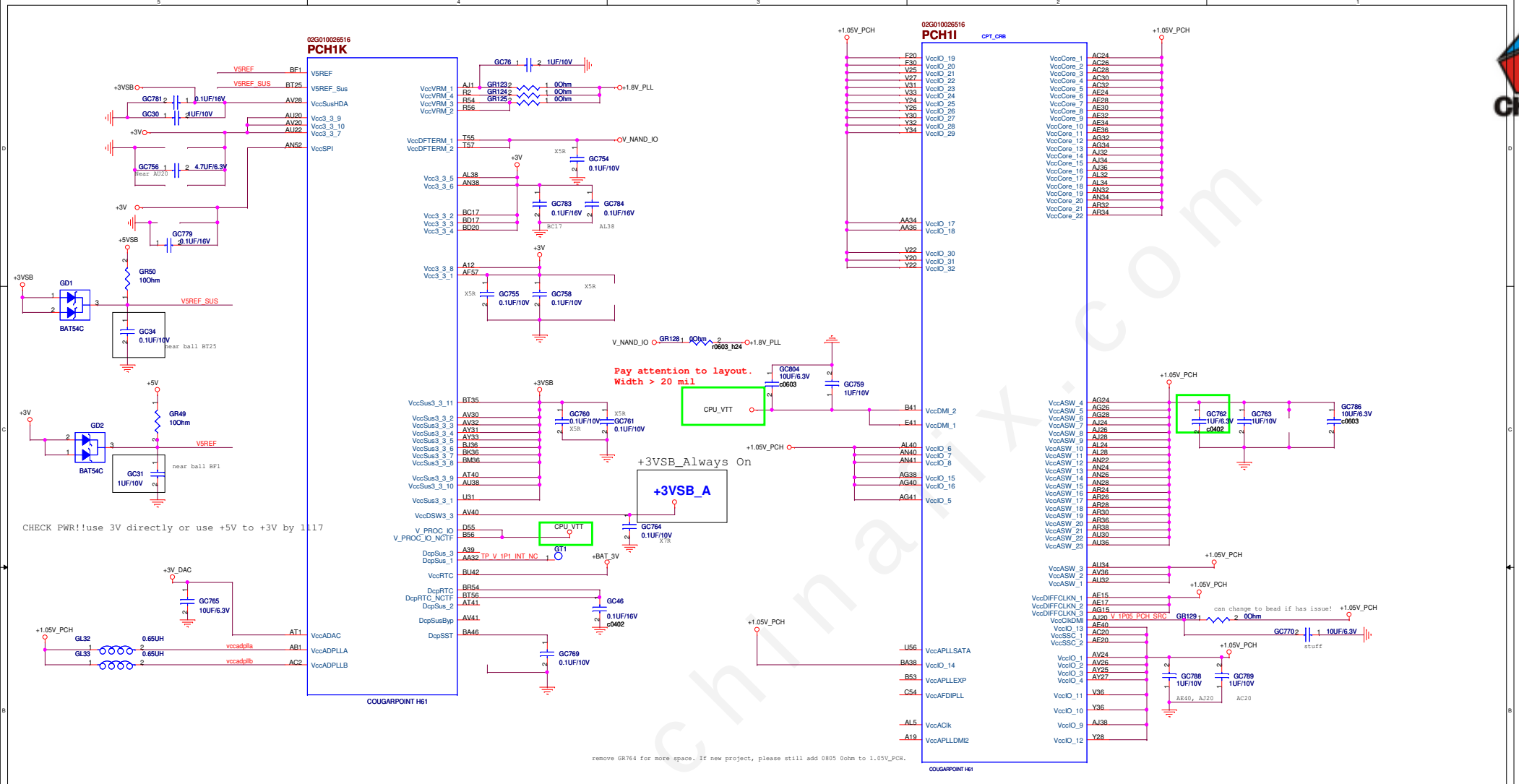

FLEX CLK HAS RULE OF USING.
SEE PDG PAGE 191 FOR DETAILS.
02G010026516
PCH1H
CPT_CRB
30 PCH_CK_33M_SIO
10 CLK_PCH_PORT80
10 PCH_CK_PCI_LB
GR736 22Ohm
GR773 22Ohm
GR770 22Ohm
AT11 CLKOUT_PCI0
AN14 CLKOUT_PCI1
AT12 CLKOUT_PCI2
AT17 CLKOUT_PCI3
AT14 CLKOUT_PCI4
AT9 CLKOUTFLEX0/GPIO64
BA5 CLKOUTFLEX1/GPIO65
AW5 CLKOUTFLEX2/GPIO66
BA2 CLKOUTFLEX3/GPIO67
23 PCH_25M
30 PCH_CK_48M_SIO
RG31 r0402 0Ohm LAN_25M
+1.05V_PCH
90.9Ohm 1% GR43
AL2 XCLK_RCOMP
AN8 REFCLK14IN
14Mhz no need to connect by using internal clock.
GR797 10KOhm
Flex 0, 1, 2, 3 : Check ME setting!!
AJ5 XTAL25_OUT
AJ3 XTAL25_IN
1MOhm GR45
GX1
25Mhz
GC12 27PF/50V
GC13 27PF/50V
CLKIN_GND1_N R27
CLKIN_GND1_P P27
CLKIN_GND0_N W53
CLKIN_GND0_P V52
GR756 GR757 GR759 GR758 10KOhm
CLKOUT_ITPXDP_N R52
CLKOUT_ITPXDP_P N52
CLKOUT_PCIE7N AE2
CLKOUT_PCIE7P AF1
CLKOUT_DMI_N P31
CLKOUT_DMI_P R31
PCH_CK_DMI# 7
PCH_CK_DMI 7
CPU
CLKOUT_DP_N N56
CLKOUT_DP_P M55
unused for PCH platform
CLKOUT_PCIE0N AE6
CLKOUT_PCIE0P AC6
PCH_ECLK_PCIE2# 27
PCH_ECLK_PCIE2 27
PCIE x1 Slot
CLKOUT_PCIE1N AA5
CLKOUT_PCIE1P W5
CLKOUT_PCIE2N AB12
CLKOUT_PCIE2P AB14
PCH_ECLK_LAN# 23
PCH_ECLK_LAN 23
LAN
CLKOUT_PCIE3N AB9
CLKOUT_PCIE3P AB8
CLKOUT_PCIE4N Y9
CLKOUT_PCIE4P Y8
CLKOUT_PCIE5N AF3
CLKOUT_PCIE5P AG2
CLKOUT_PCIE6N AB3
CLKOUT_PCIE6P AA2
CLKOUT_PEG_A_N AG8
CLKOUT_PEG_A_P AG9
PCH_ECLK_X16# 27
PCH_ECLK_X16 27
PCIE x16 Slot
CLKOUT_PEG_B_N AE12
CLKOUT_PEG_B_P AE11
COUGARPOINT H61
H67M-ITX
ASRock Title :PCH - CLK
ASRock Inc.
Engineer: Isaac Lee
Size B
Project Name H67M-ITX
Rev 1.03
Date: Tuesday, May 07, 2013
Sheet 16 of 47



H67M-ITX

ASRock Title : PCH - Power

ASRock Inc. Engineer: Isaac Lee

Size	Project Name	Rev
C	H67M-ITX	1.03

Date: Wednesday, December 19, 2012 Sheet 17 of 47

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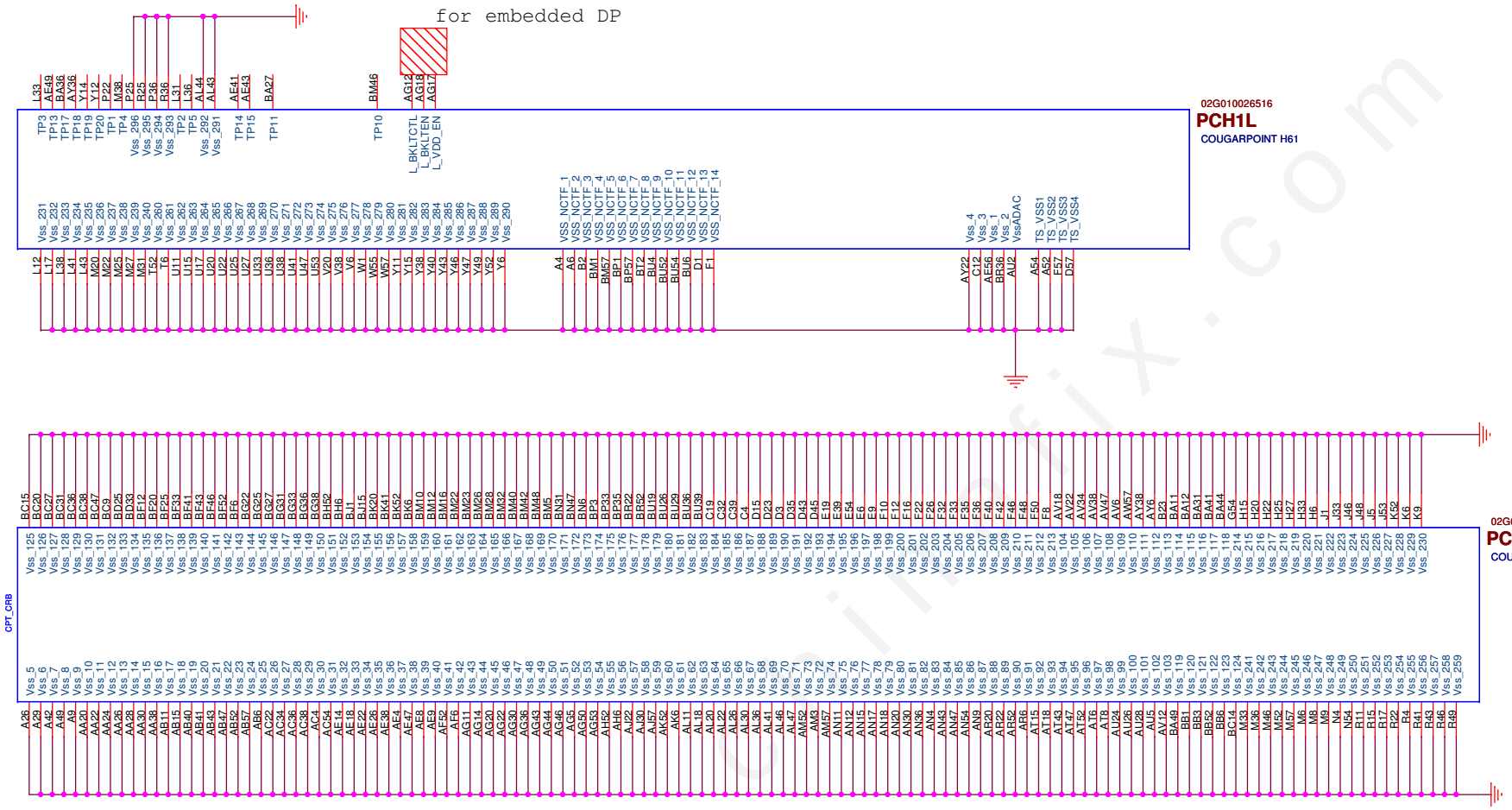
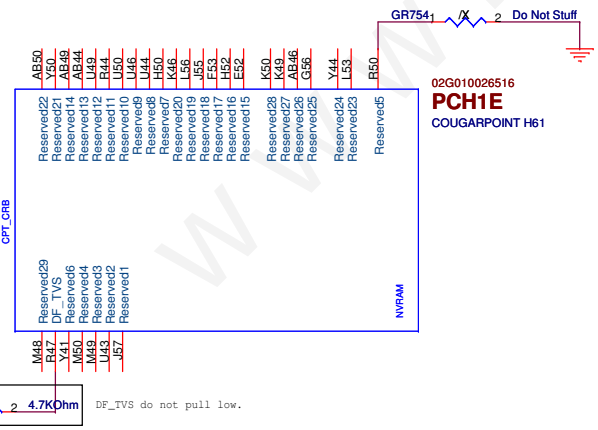
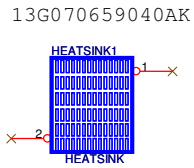






H67M-ITX

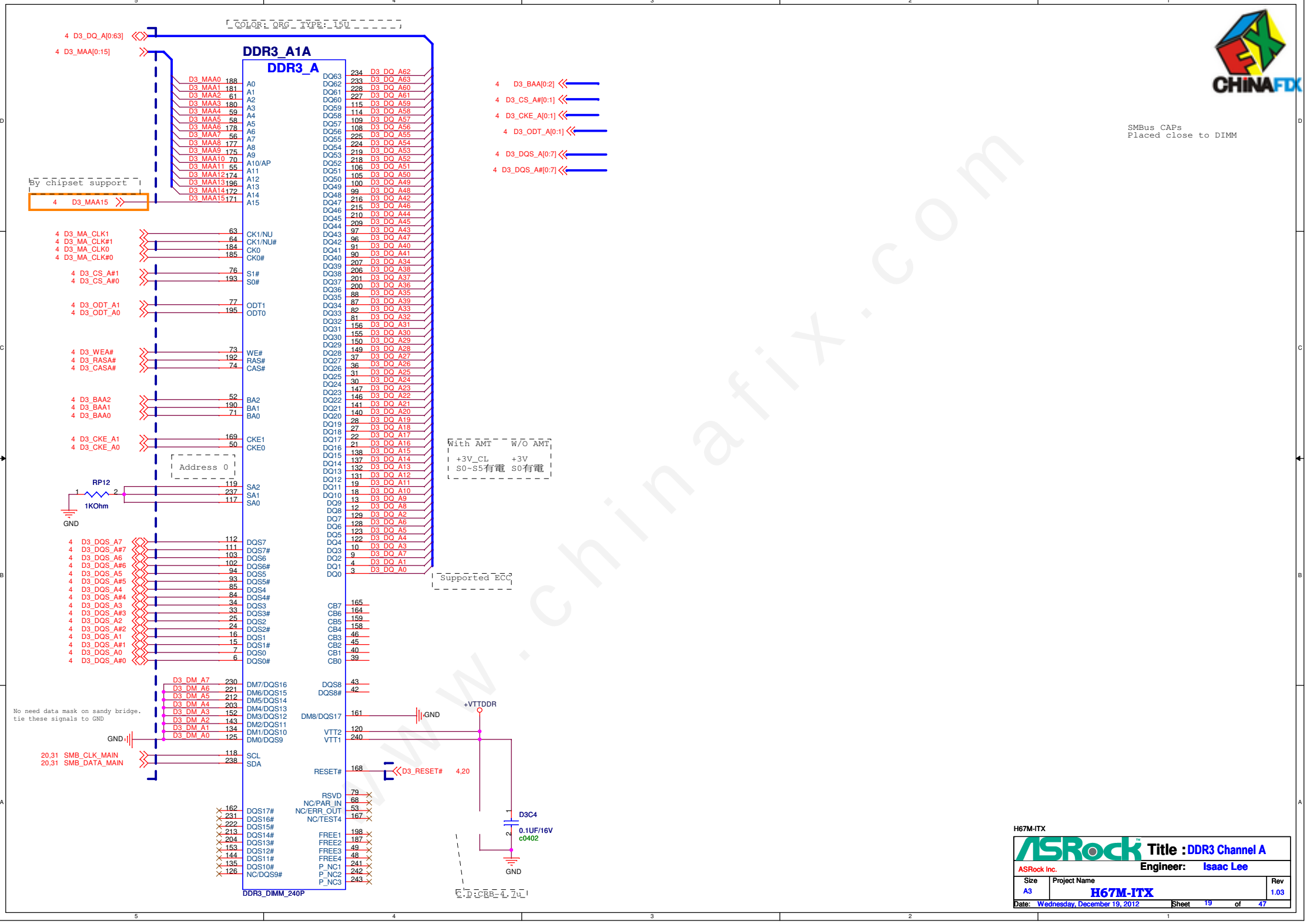
ASRock Inc.

Title : PCH - GND

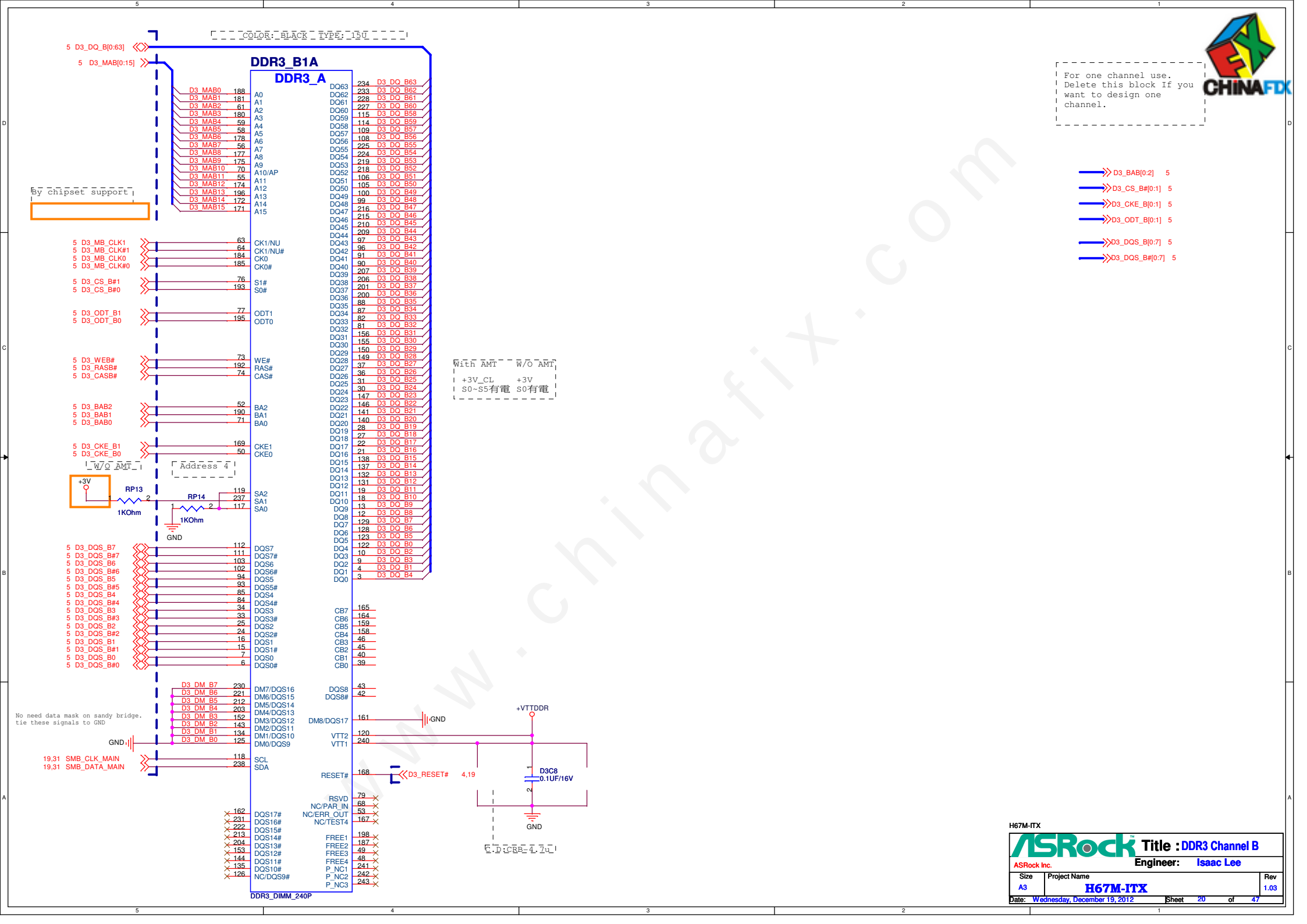
Engineer: Isaac Lee

Size	Project Name	Rev
A3	H67M-ITX	1.03

Date: Wednesday, December 19, 2012 Sheet 18 of 47



www.chinafix.com



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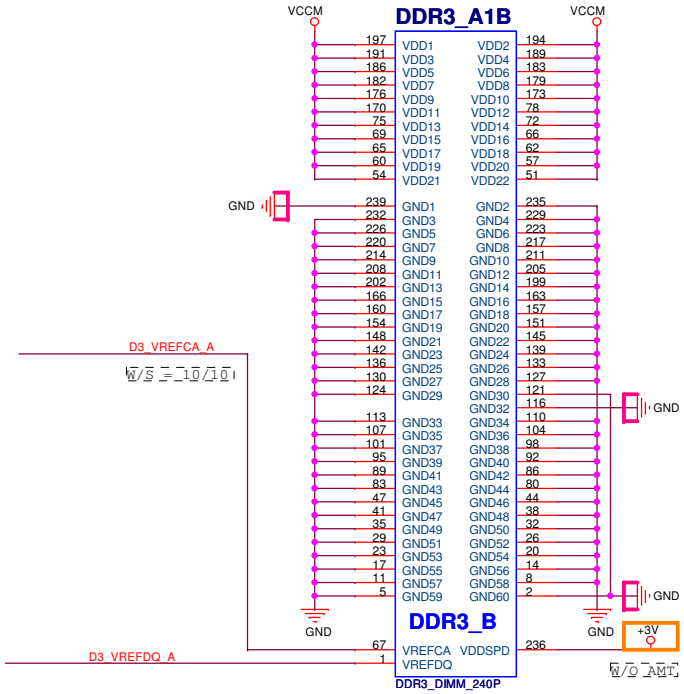
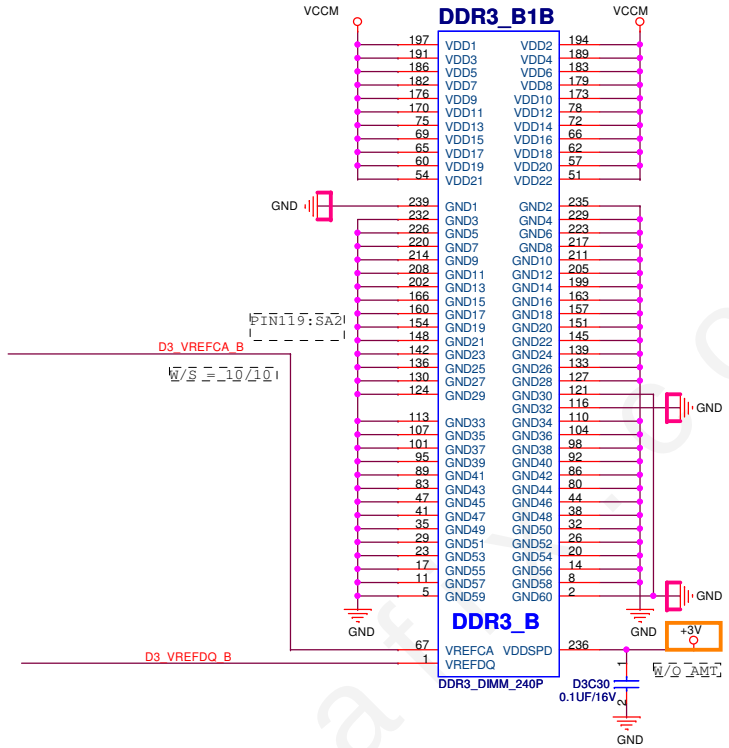
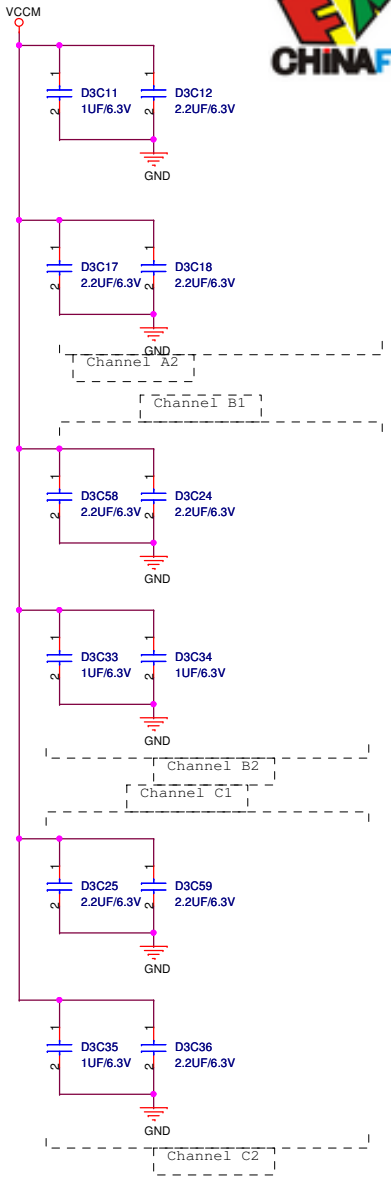
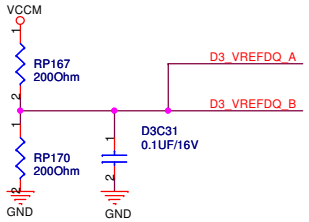
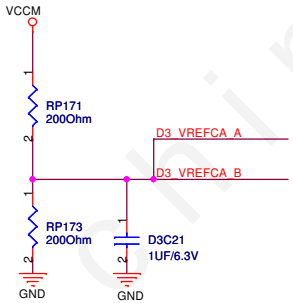




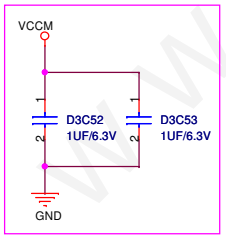




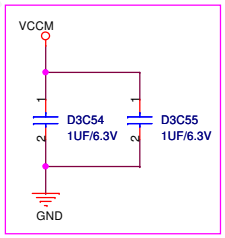


c.w. huang:Add 10uF cap. to improve DDR3 over clock.

channel A



channel B



With AMT	W/O AMT
+3V_CL	+3V
S0~S5有電	S0有電

H67M-ITX

ASRock Inc.

Title : DDR3 (Power)

Engineer: Isaac Lee

Size	Project Name	Rev
A3	H67M-ITX	1.03

Date: Wednesday, December 19, 2012 Sheet 21 of 47

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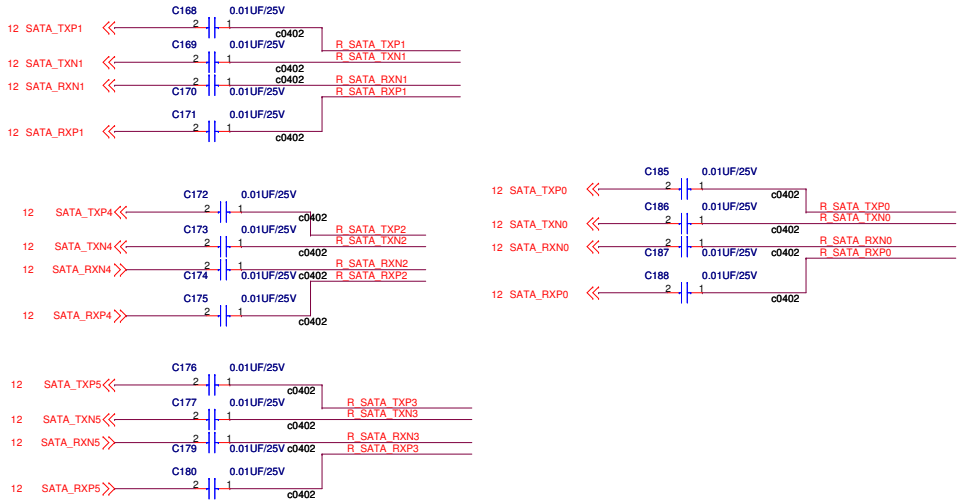
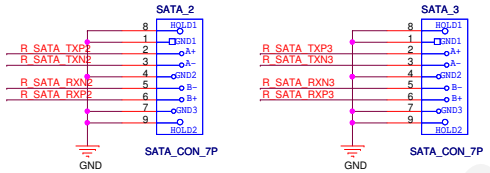
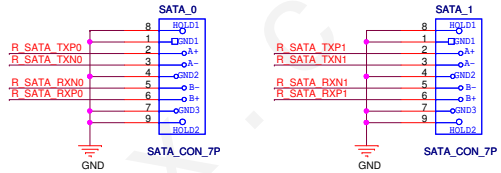


INTEL SATA2

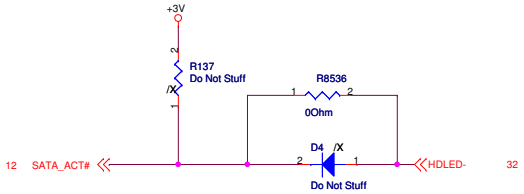


INTEL SATA3



SATA3 & SATA LED

1.00 Internal Pull UP
1.00 If need pul up, check +3.3V or +5V



Check SATA Port Name with leaders!!!

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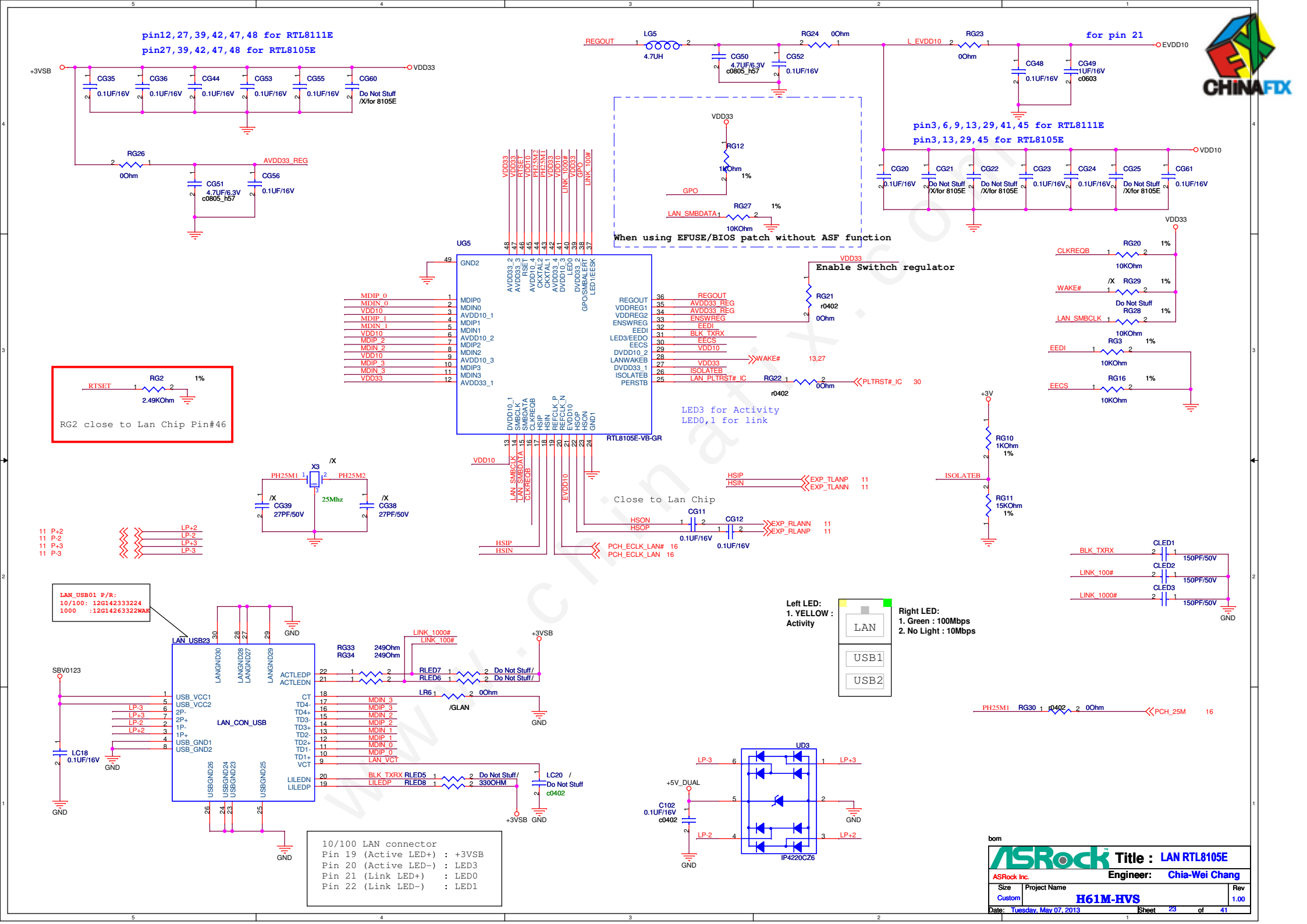
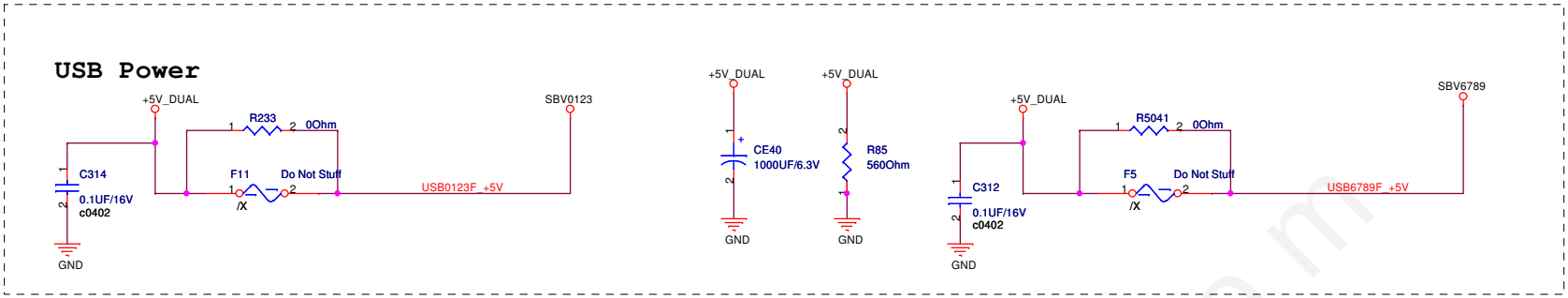
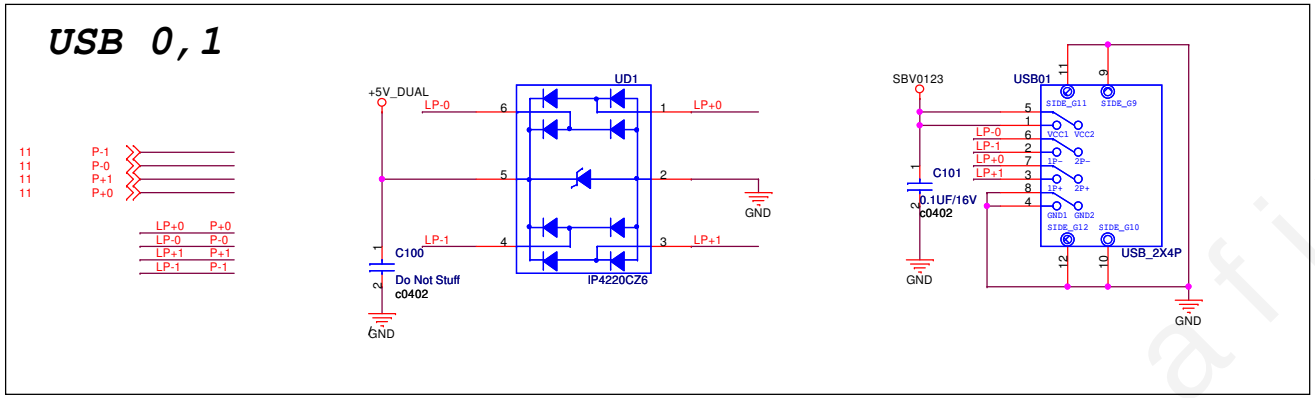
H67M-ITX

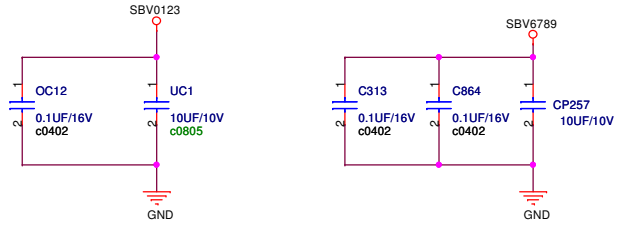
ASRock Inc.	Title : SATA3/SATA2 / ESATA	
	Engineer: Isaac Lee	
Size: Custom	Project Name: H67M-ITX	Rev: 1.03
Date: Tuesday, May 07, 2013	Sheet 22 of 47	

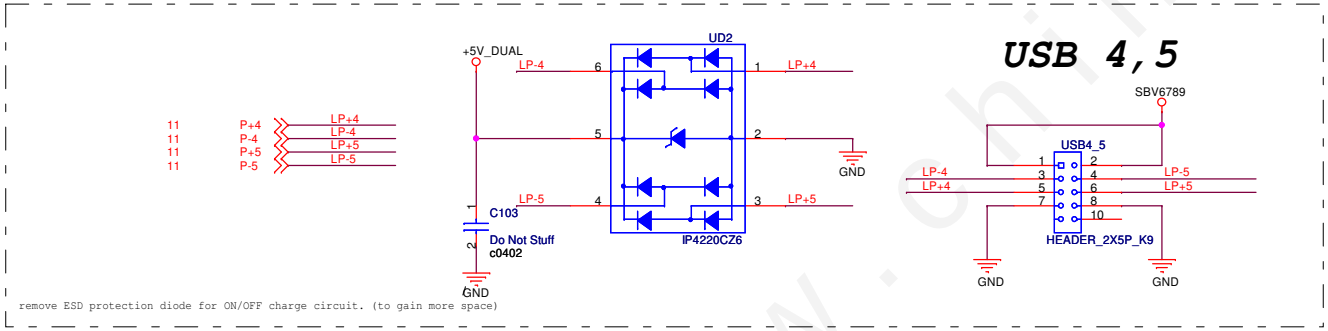


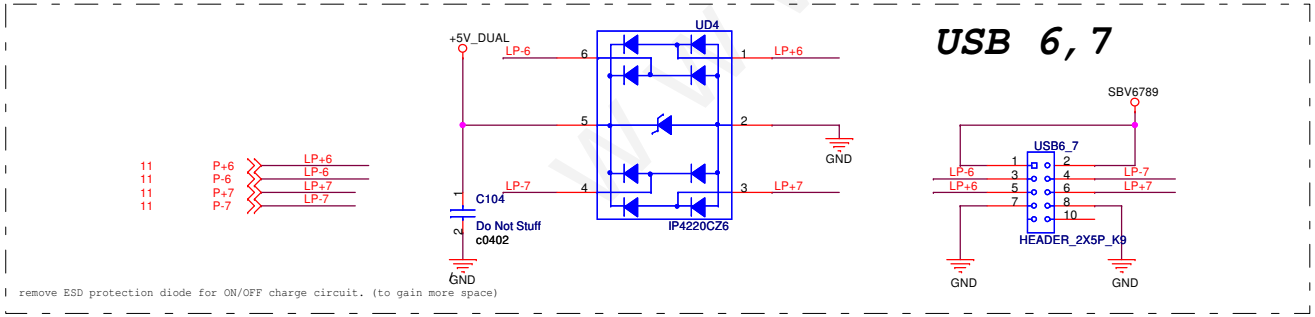
www.chinafix.com











H67M-ITX

ASRock Inc.

Title : USB Port

Engineer: Isaac Lee

Size	Project Name	Rev
A3	H67M-ITX	1.03

Date: Wednesday, December 19, 2012 Sheet 25 of 47

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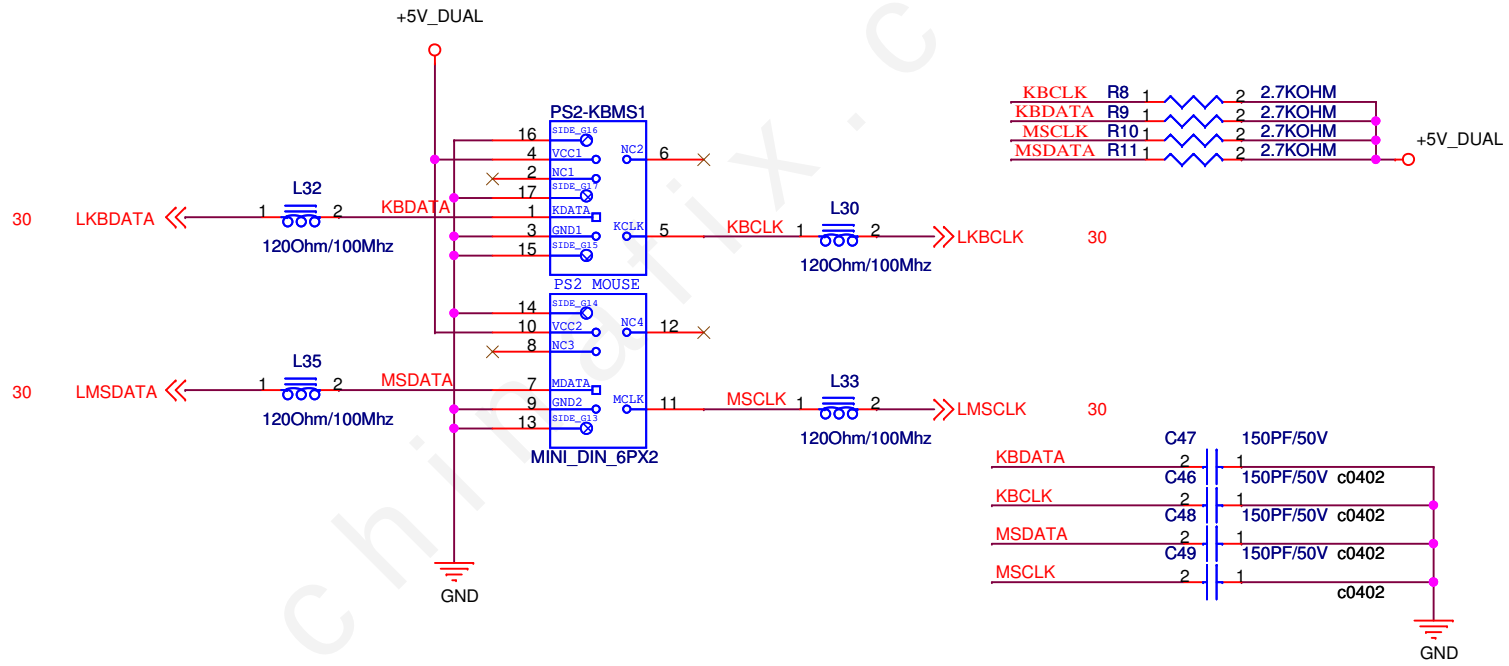
*Modify LMSCLK & LKBDATA



remove ESD protection diode for ON/OFF charge circuit. (to gain more space)

H67M-ITX

ASRock Inc.	Title : KB & MS	
	Engineer: Isaac Lee	
Size A4	Project Name H67M-ITX	Rev 1.03
Date: Wednesday, December 19, 2012	Sheet 26 of 47	

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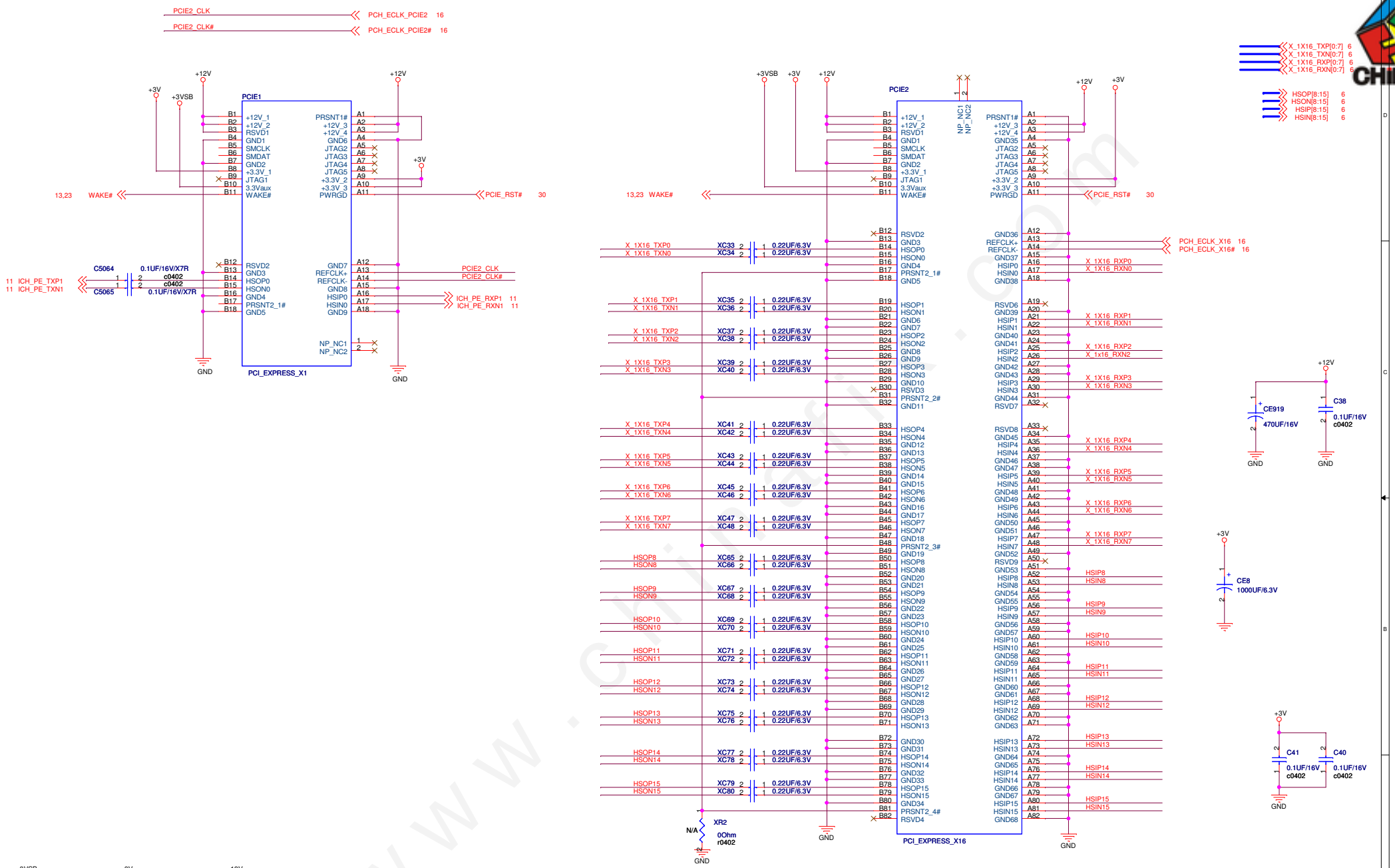


bom

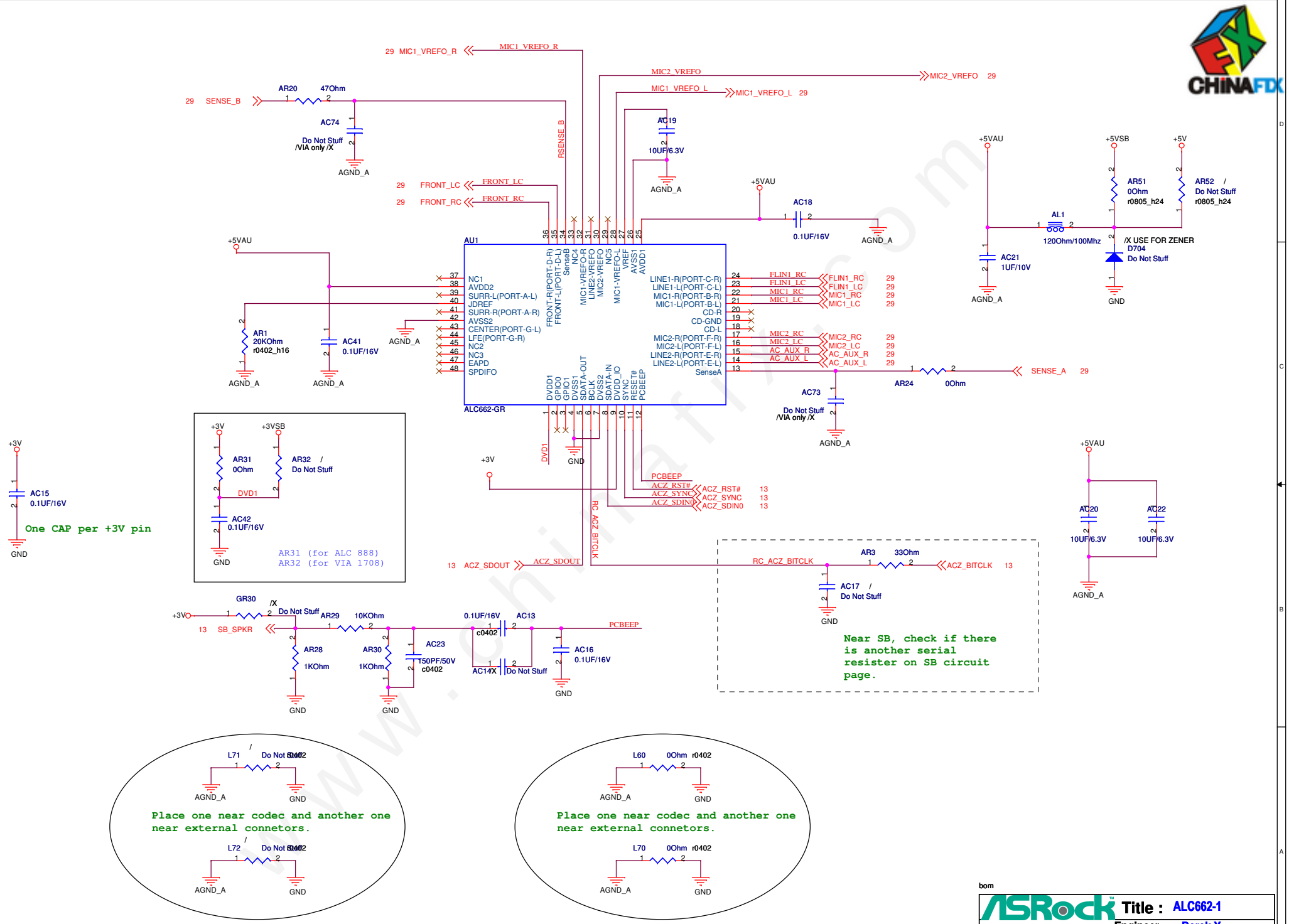
ASRock Inc.

Title : PClex1

Engineer: Chia-Wei Chang

Size	Project Name	Rev
Custom	H61M-HVS	1.00

Date: Tuesday, May 07, 2013 Sheet 27 of 41



bom

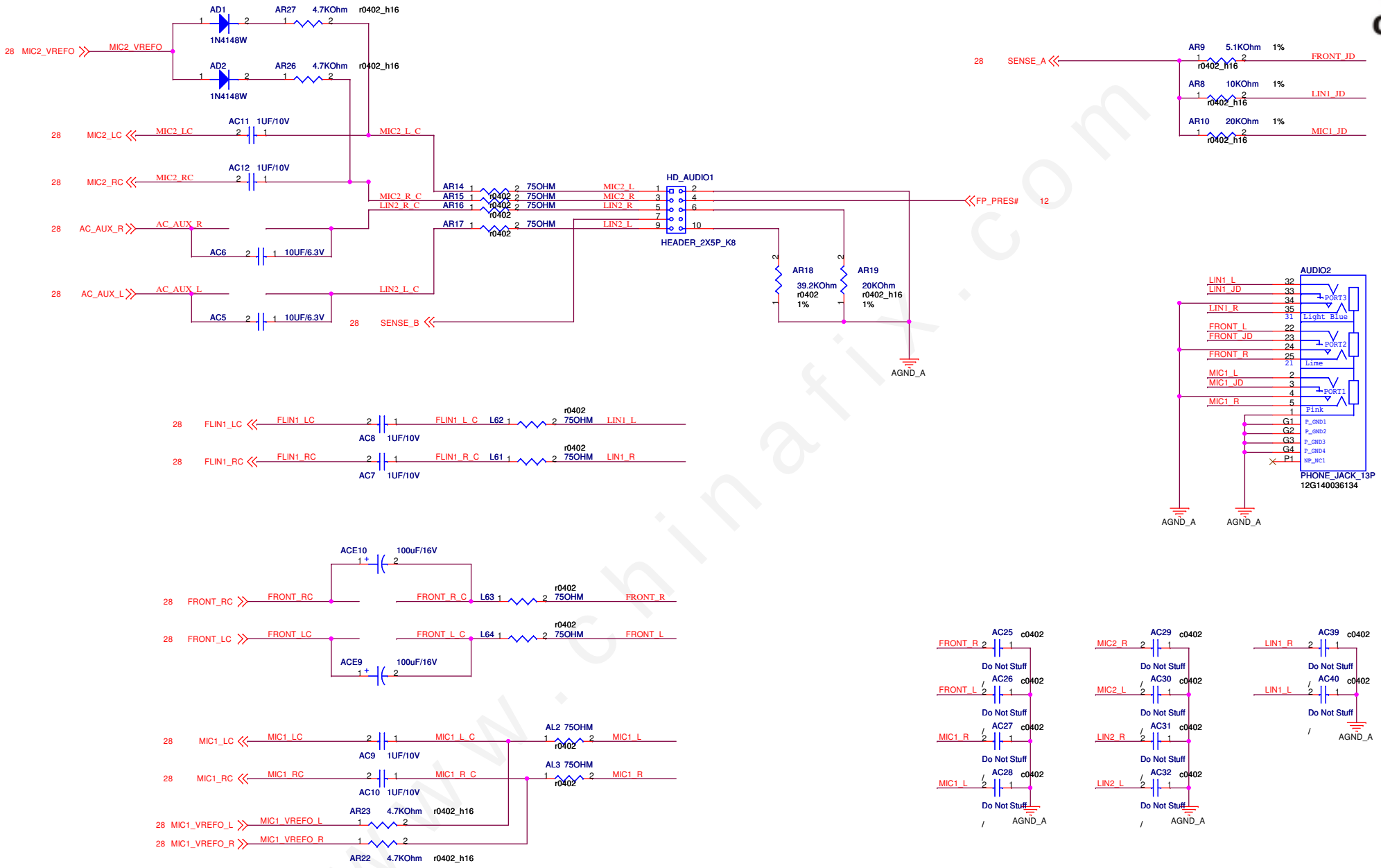
ASRock Inc.

Title : ALC662-1

Engineer: Derek Y

Size	Project Name	Rev
A3	847PV3	1.00

Date: Tuesday, May 07, 2013 Sheet 28 of 41



bom

ASRock Inc.	Title : ALC662-2	
	Engineer: Derek Y	
Size A3	Project Name 847PV3	Rev 1.00
Date: Tuesday, May 07, 2013	Sheet 29 of 41	

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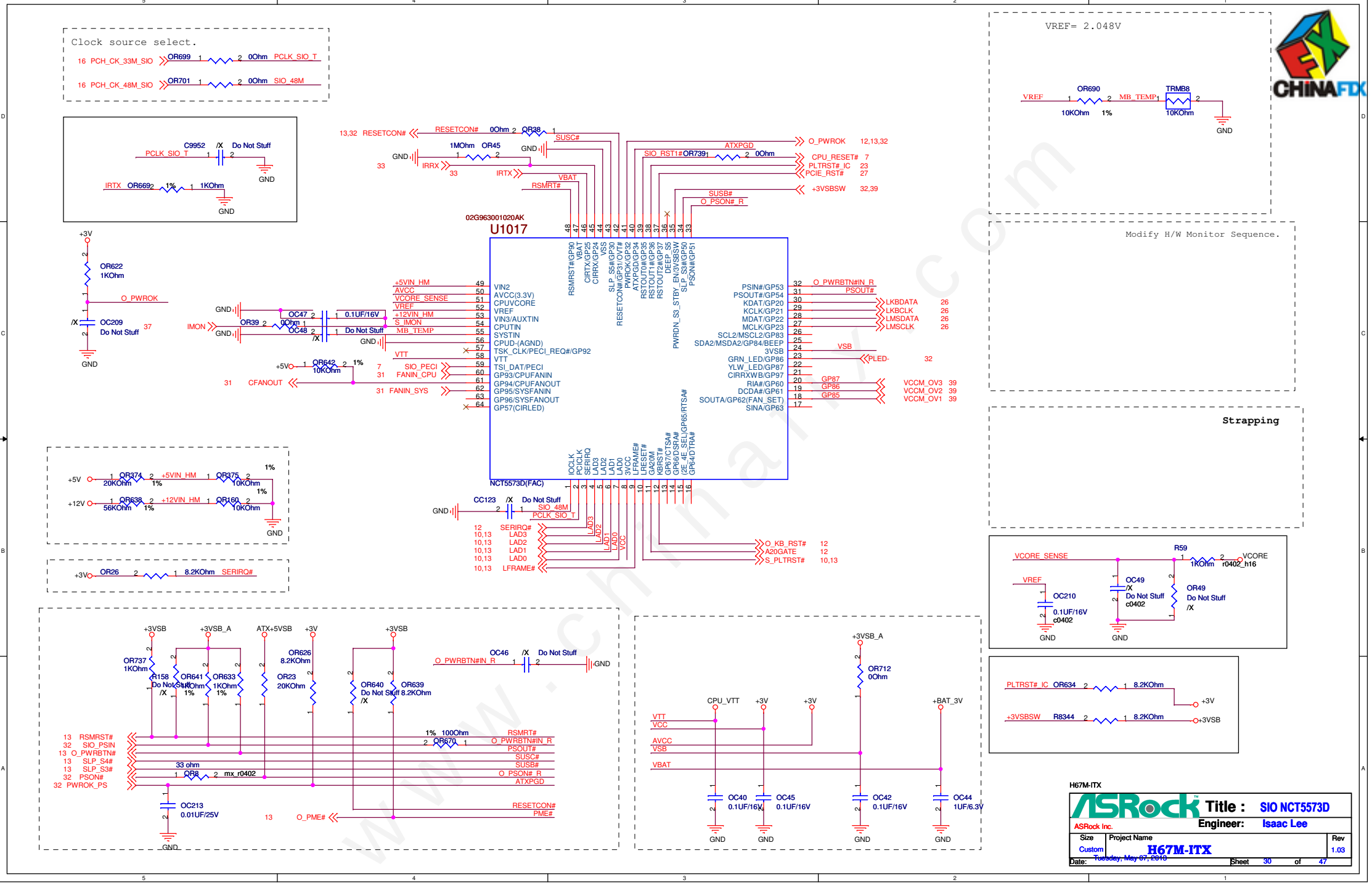

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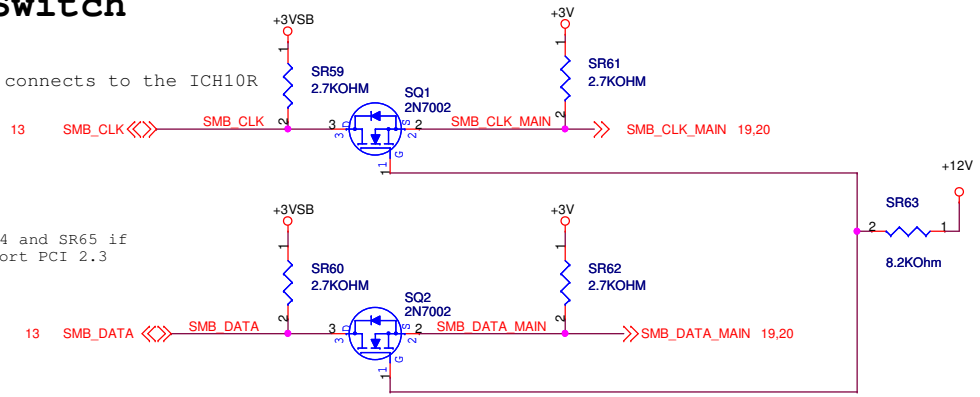
1.00 SMBus connect to two kind of devices, one use Main power, another use Standby power, so use this switch circuit to isolate those two device.
SMB_CLK and SMB_DATA for Standby device.
SMB_CLK_MAIN and SMB_DATA_MAIN for Main power device.

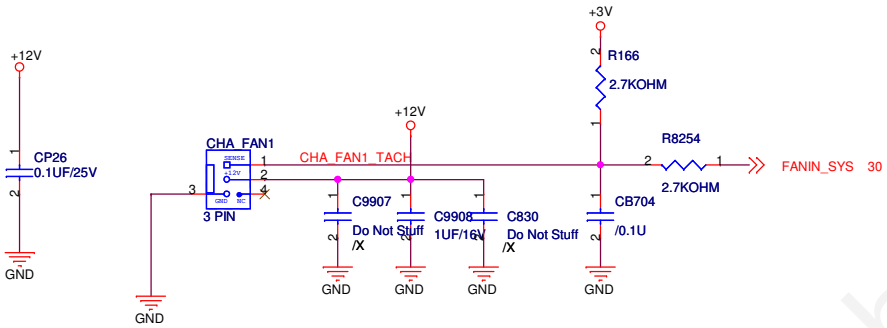
SMBus Switch

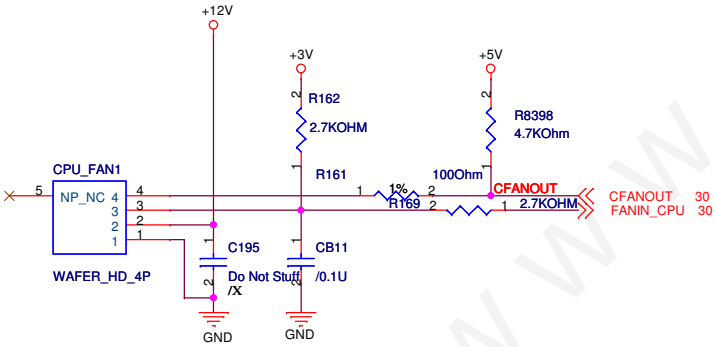
SMB_CLK and SMB_DATA connects to the ICH10R



Mount those SR64 and SR65 if we want to support PCI 2.3

SMB_CLK_PCI and SMB_DATA_PCI connects to the PCIE slot





H67M-ITX

ASRock Inc.	Title : SMBUS SWITCH,FAN	
	Engineer: Isaac Lee	
Size B	Project Name H67M-ITX	Rev 1.03
Date: Tuesday, May 07, 2013	Sheet 31 of 47	

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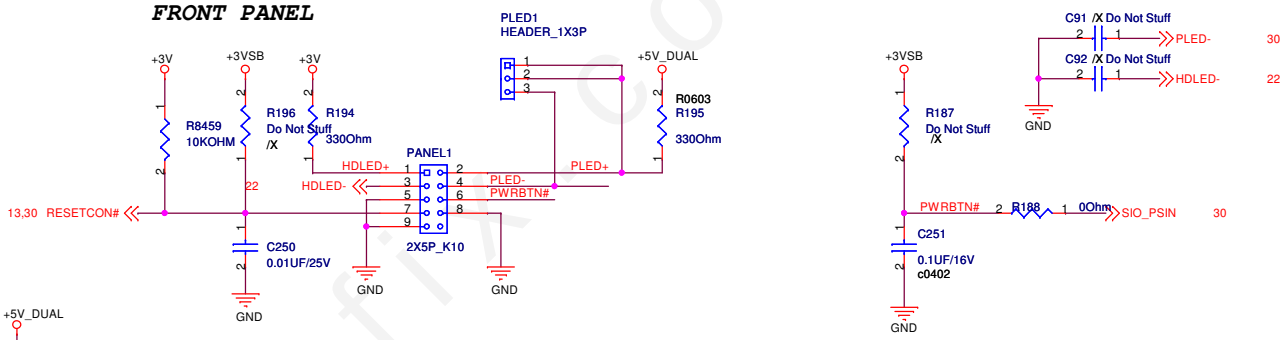
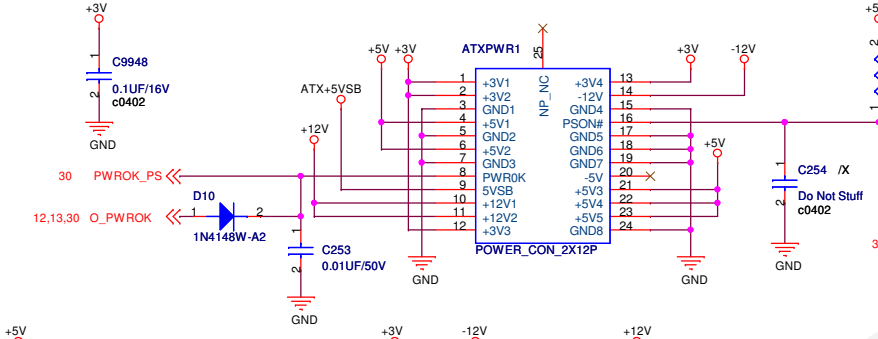
RING_IN

FRONT PANEL

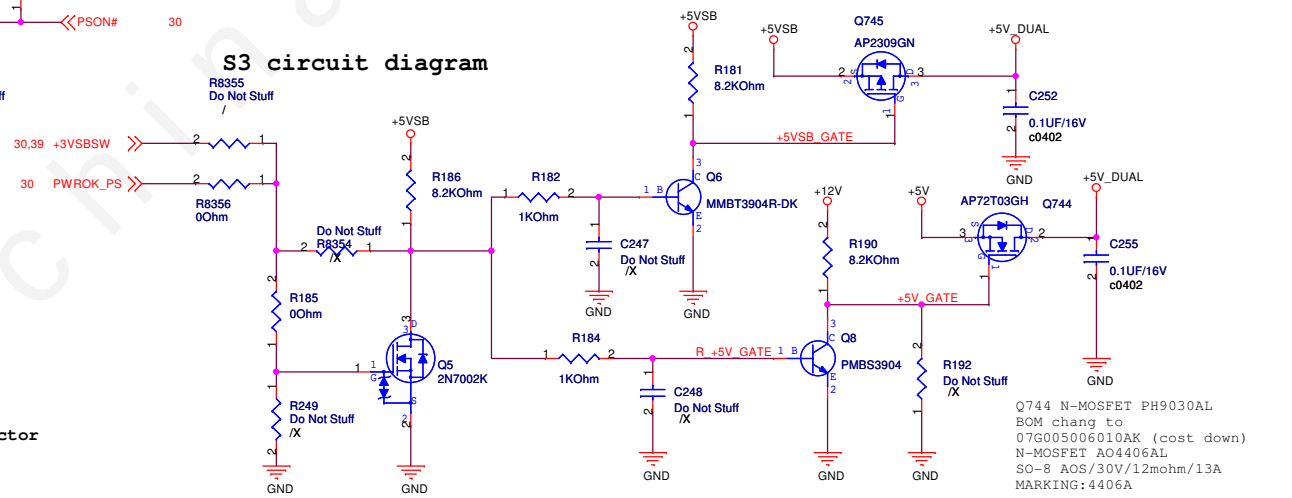


ATXPWR CONN



*Around the ATX Power Connector

S3 circuit diagram



Q744 N-MOSFET PH9030AL
BOM chang to
07G005006010AK (cost down)
N-MOSFET AO4406AL
SO-8 AOS/30V/12mohm/13A
MARKING:4406A

Logic IC : R190 = 2.7K, Q8 = 2N7002
BJT : R190 = 8.2K, Q8 = 3904, R192
= uninstall

+5VSB
C275
0.1UF/16V
c0402
GND

bom

ASRock Inc.	Title : POK_DUALSW_ENASUS	
	Engineer: Isaac Lee	
Size A3	Project Name H67M-ITX	Rev 1.03
Date: Tuesday, May 07, 2013	Sheet 32 of 41	

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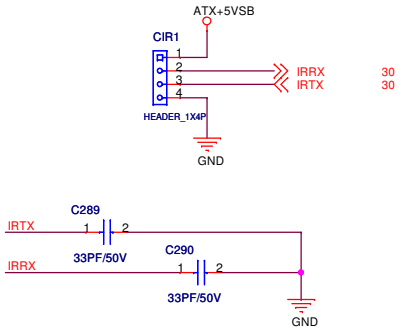
COM

IR

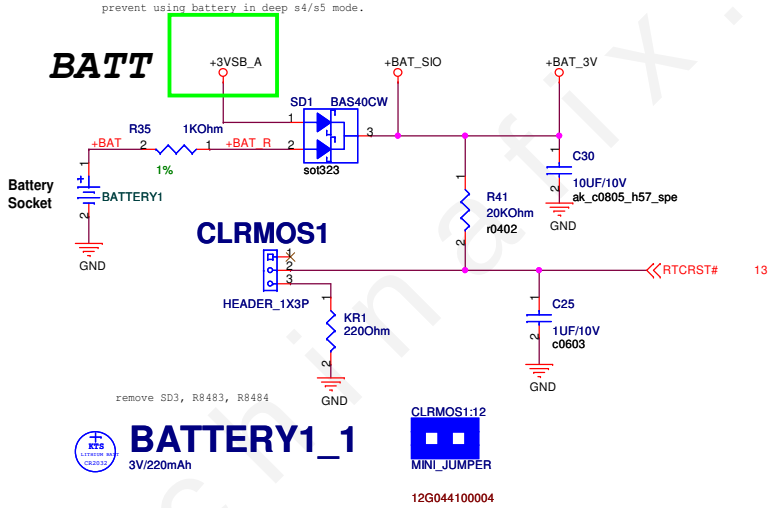


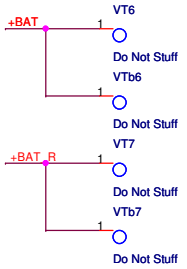
Wifi

prevent using battery in deep s4/s5 mode.

prevent using battery in deep s4/s5 mode.

BATT





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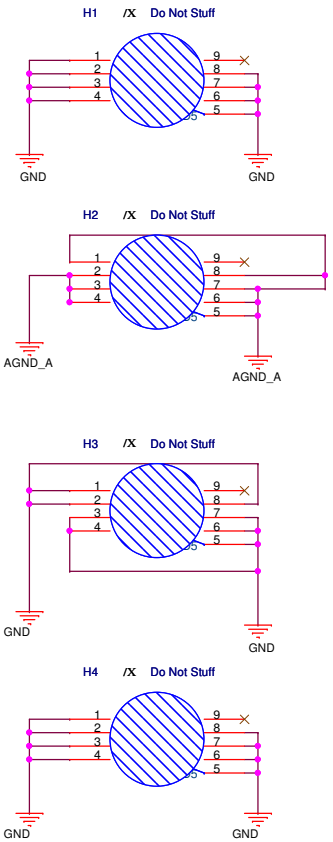
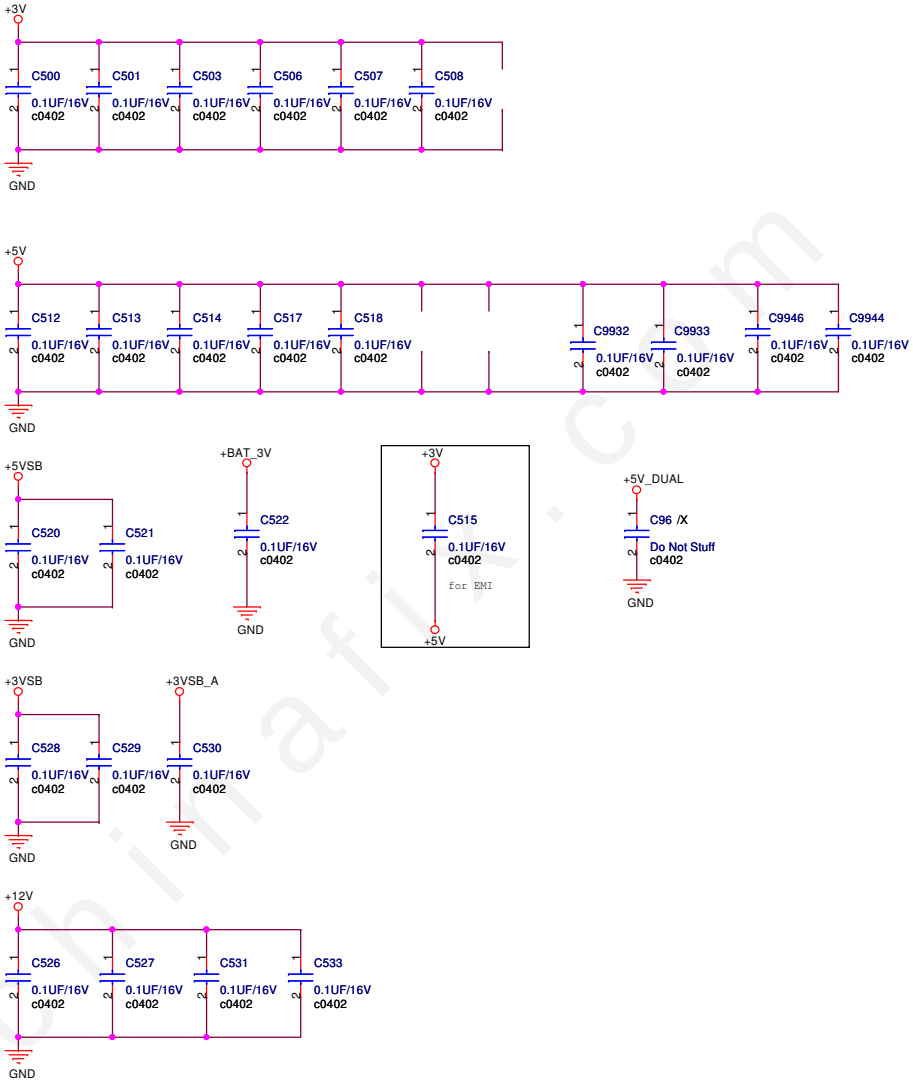
H67M-ITX

ASRock Inc.	Title : IO CONNECTOR	
	Engineer: Isaac Lee	
Size A3	Project Name H67M-ITX	Rev 1.03
Date: Tuesday, May 07, 2013	Sheet 33 of 47	

SCREW_HOLE





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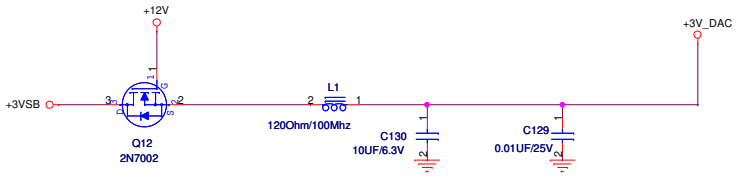
H67M-ITX

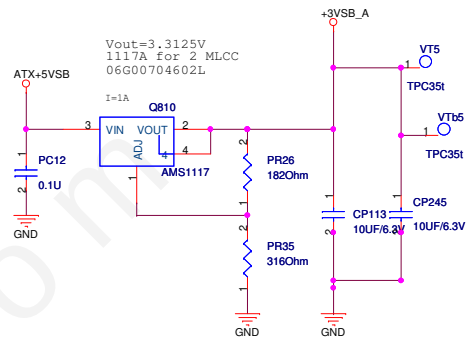
ASRock Inc.	Title : MECHANICAL	
	Engineer: Isaac Lee	
Size A3	Project Name H67M-ITX	Rev 1.03
Date: Wednesday, December 19, 2012	Sheet 34 of 47	

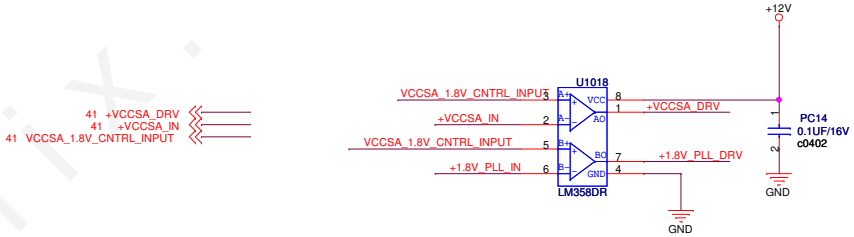
Soft Start - PCH

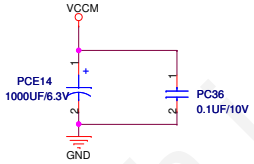
+3.3V_DAC



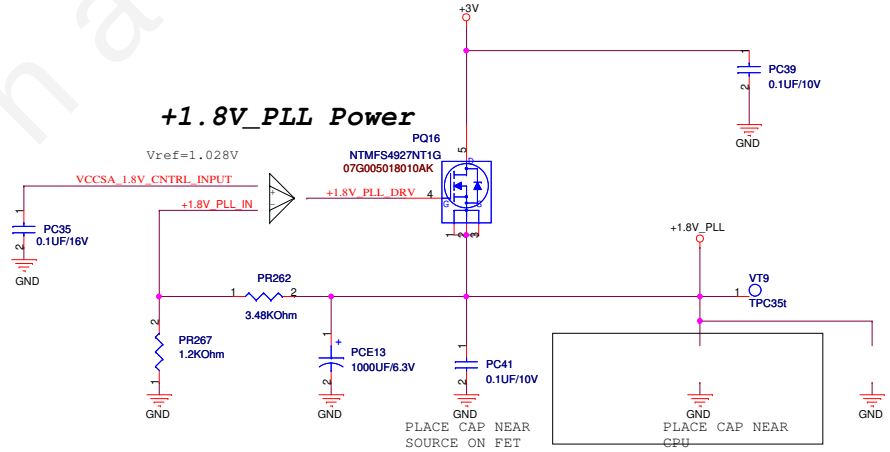
+3VSB_A

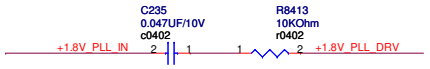






+1.8V_PLL Power





bom

ASRock Inc.

Title : DC_DC

Engineer: Isaac Lee

Size	Project Name	Rev
Custom	H67M-ITX	1.03

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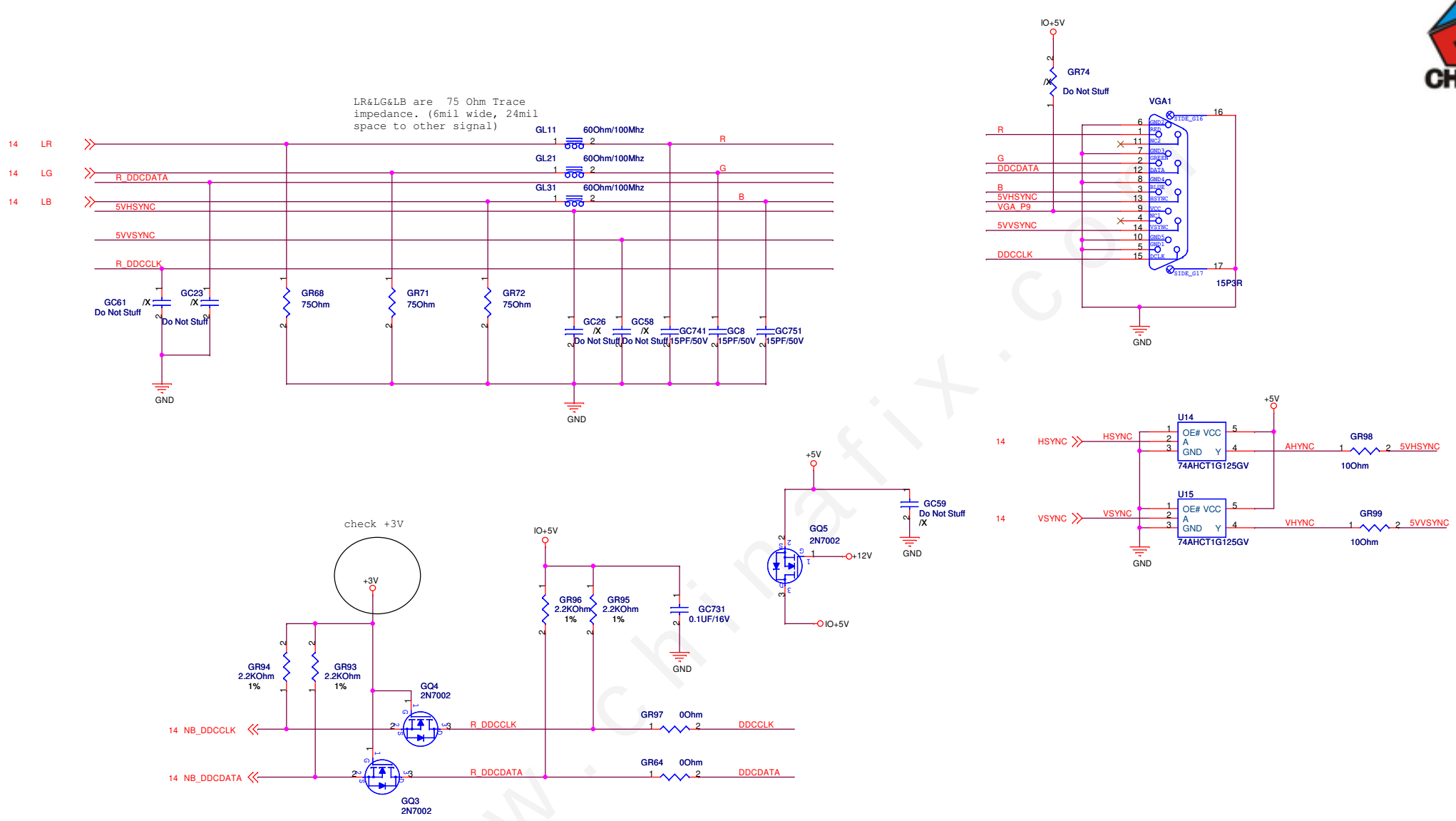

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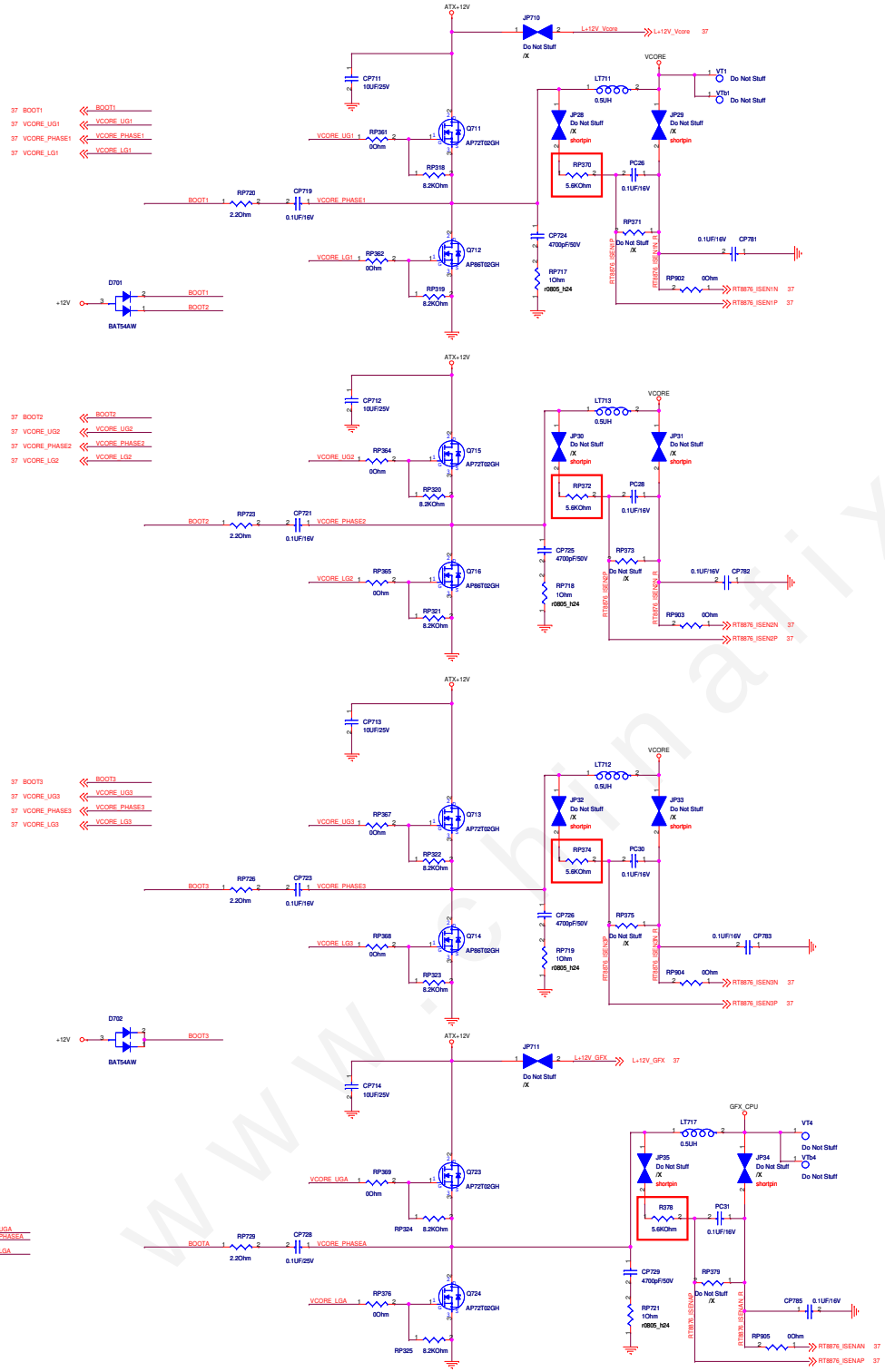
H67M-ITX

ASRock Title : VGA CONNECTOR

ASRock Inc. Engineer: Isaac Lee

Size	Project Name	Rev
A3	H67M-ITX	1.03

Date: Tuesday, May 07, 2013 Sheet 35 of 47



bom

ASRock Inc.

Title : Vcore MOS

Engineer: Kwela Chiu

Size	Project Name	Rev
Custom	Thin Mini-ITX	1.00

Date: Wednesday, December 19, 2012 Sheet 36 of 41

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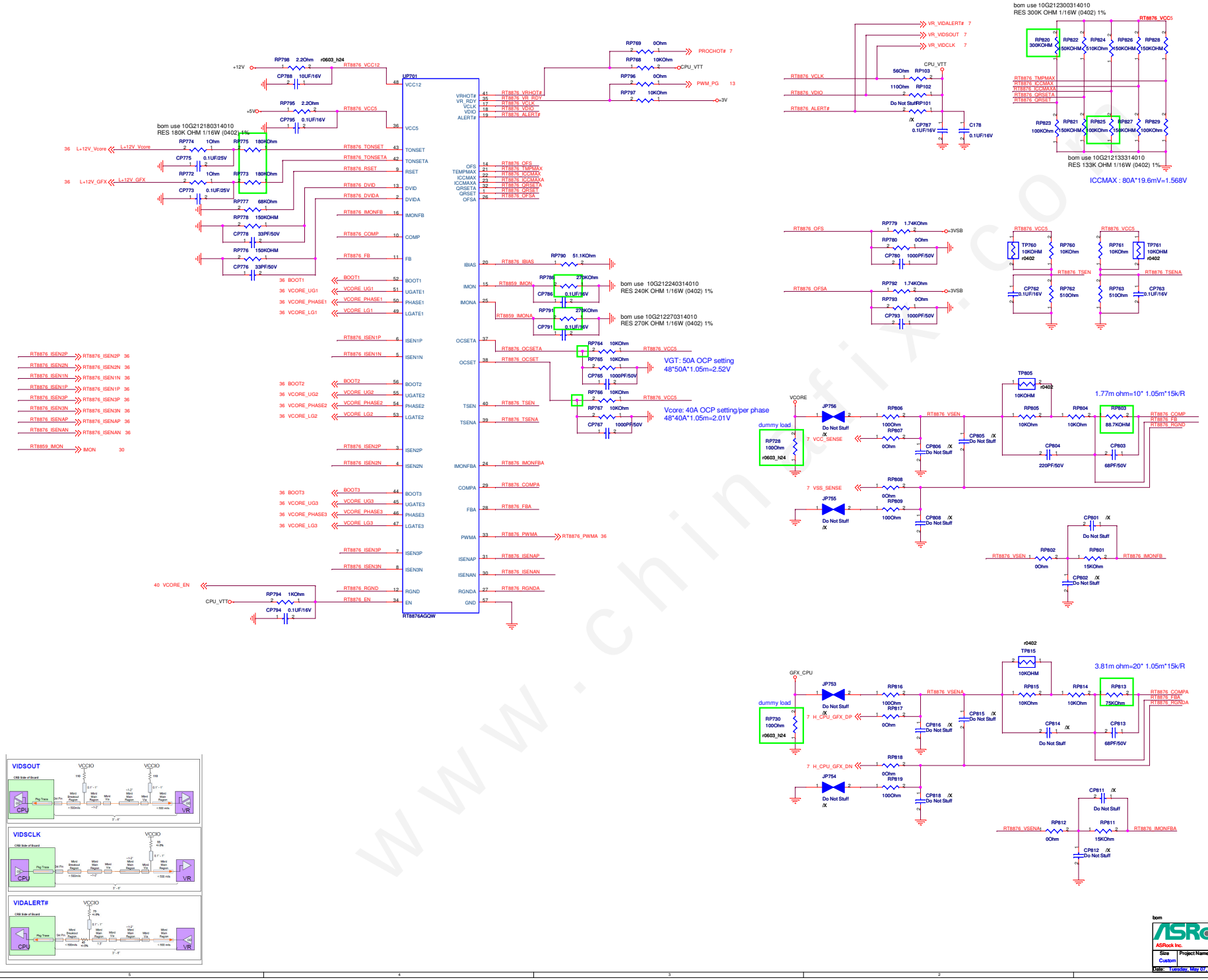

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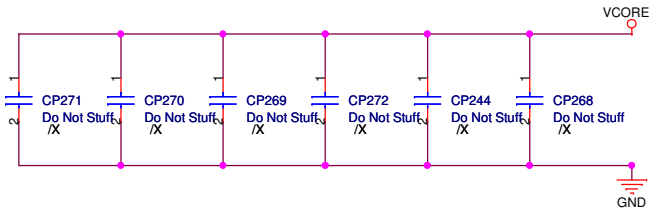
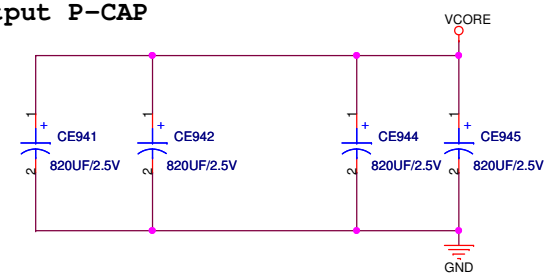
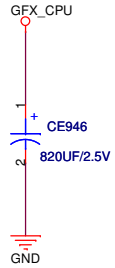
ASRock Inc.	Title : PWM RT8859		
	Engineer: Kwela Chiu		
Size: Custom	Project Name: Thin Mini-ITX		Rev: 1.00
Date: Tuesday, May 07, 2013	Sheet 37 of 41		

Vcore output P-CAP



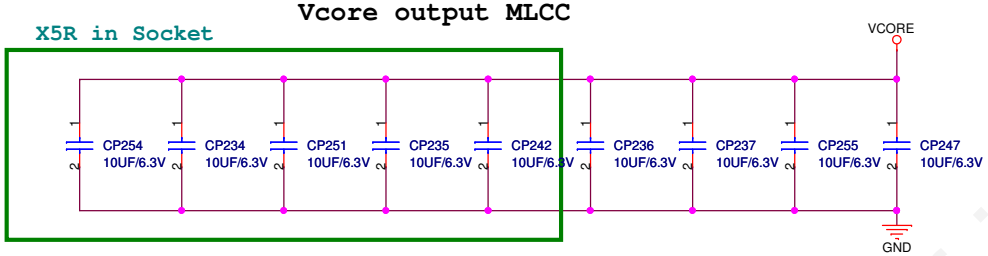


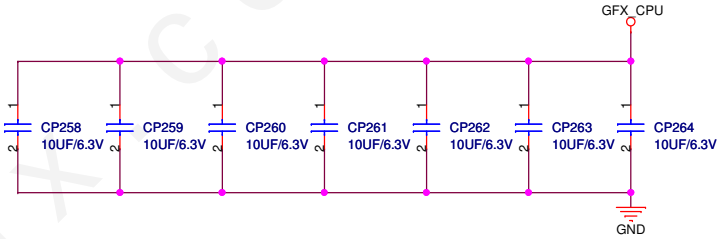
GFX output P-CAP

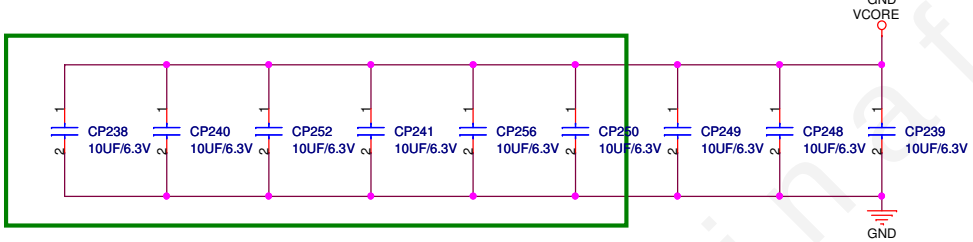


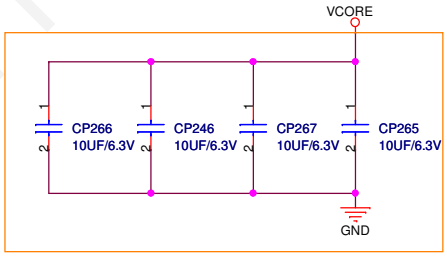
Vcore output MLCC

X5R in Socket



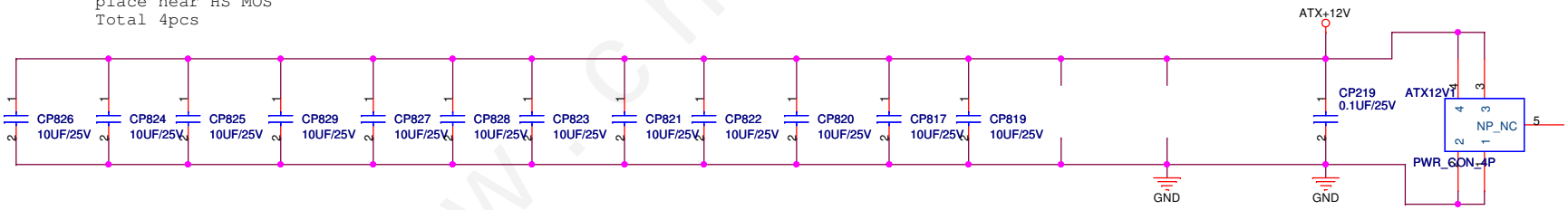






Vcore Input P-CAP

place near HS MOS
Total 4pcs



bom

ASRock Inc.	Title : VCORE	
	Engineer: Isaac Lee	
Size B	Project Name H67M-ITX	Rev 1.03
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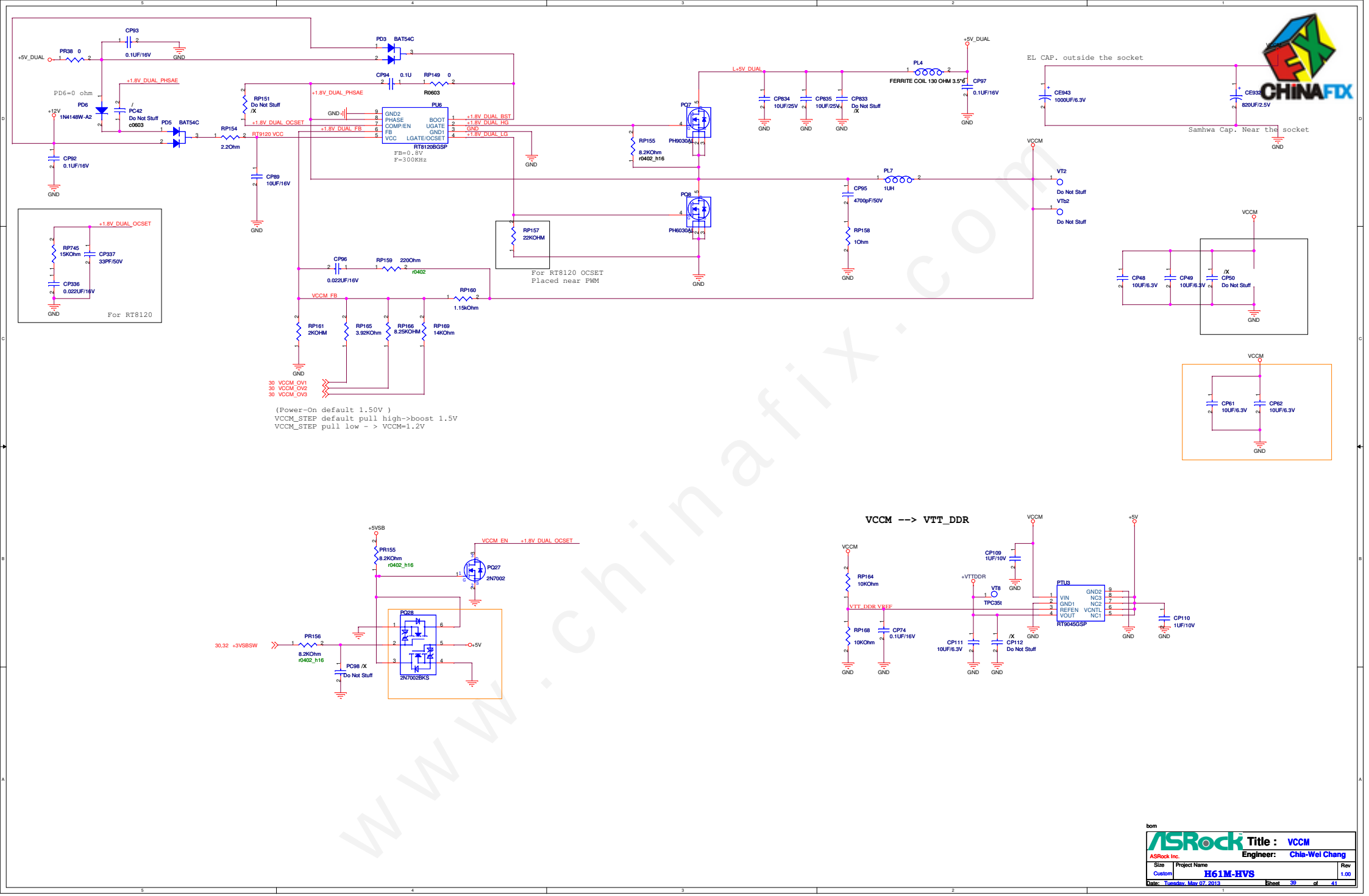

bom

ASRock Inc.	Title : VCCM	
	Engineer: Chia-Wei Chang	
Size: Custom	Project Name: H61M-HVS	Rev: 1.00
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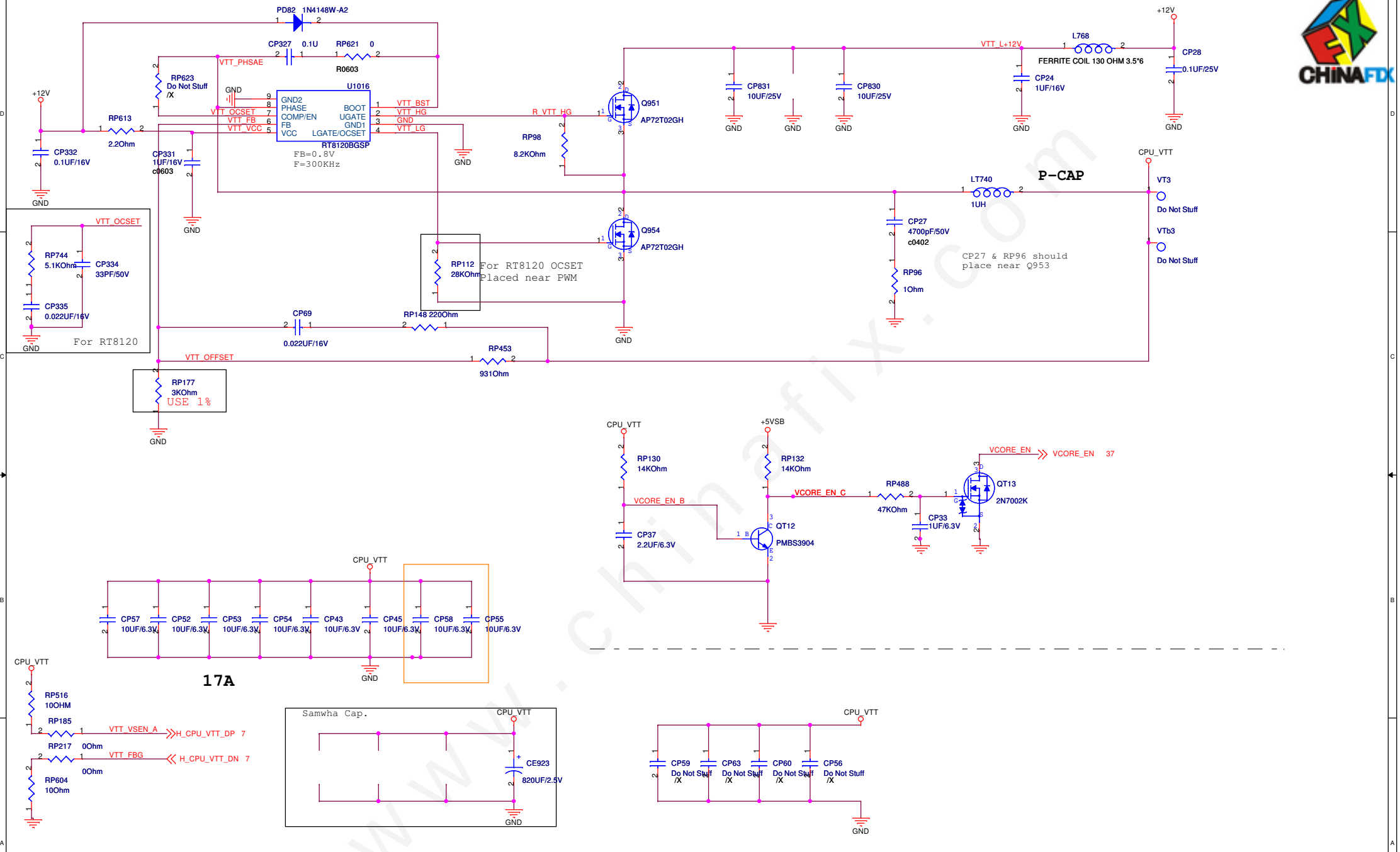

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ASRock Inc.	Title : VTT	Engineer: Chia-Wei Chang
Size A3	Project Name H61M-HVS	Rev 1.00
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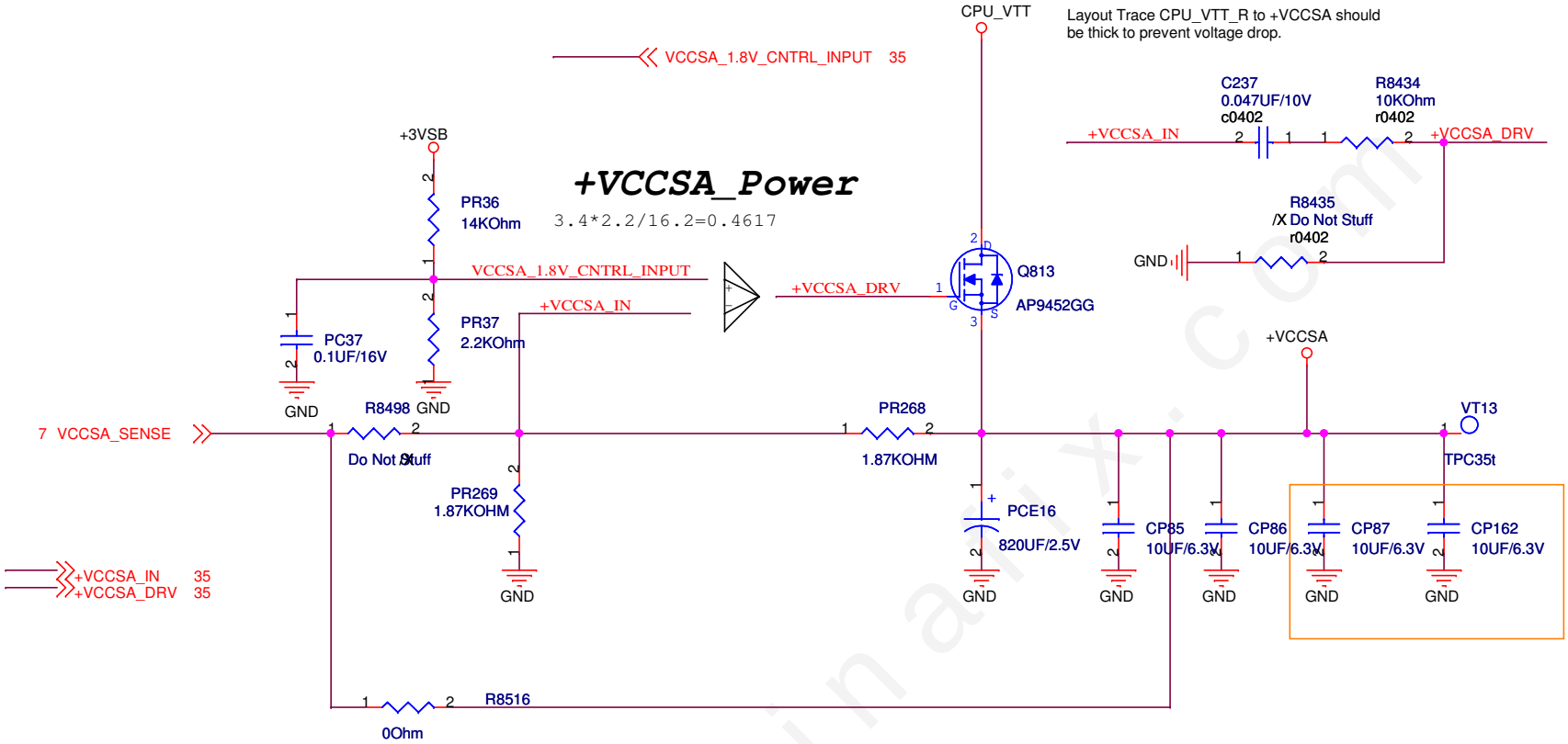

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ASRock Inc.	Title : VTT	
	Engineer: Chia-Wei Chang	
Size: Custom	Project Name: H61M-HVS	Rev: 1.00
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